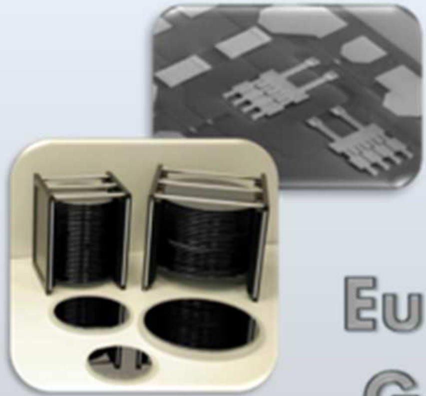
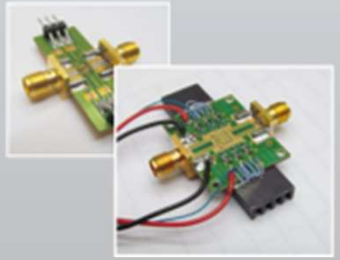
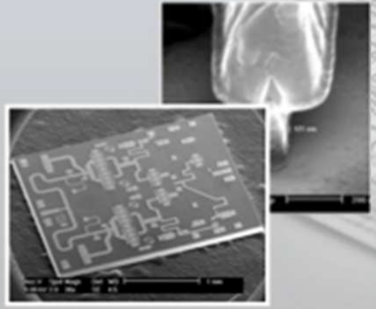
OMMIC *Innovating with III-V's*

OMMIC



Europe's Independent GaAs InP GaN MMIC Supplier





Mixed D/A ED02AH process for radar control functions and new GaN/Si for hyper-frequency power applications

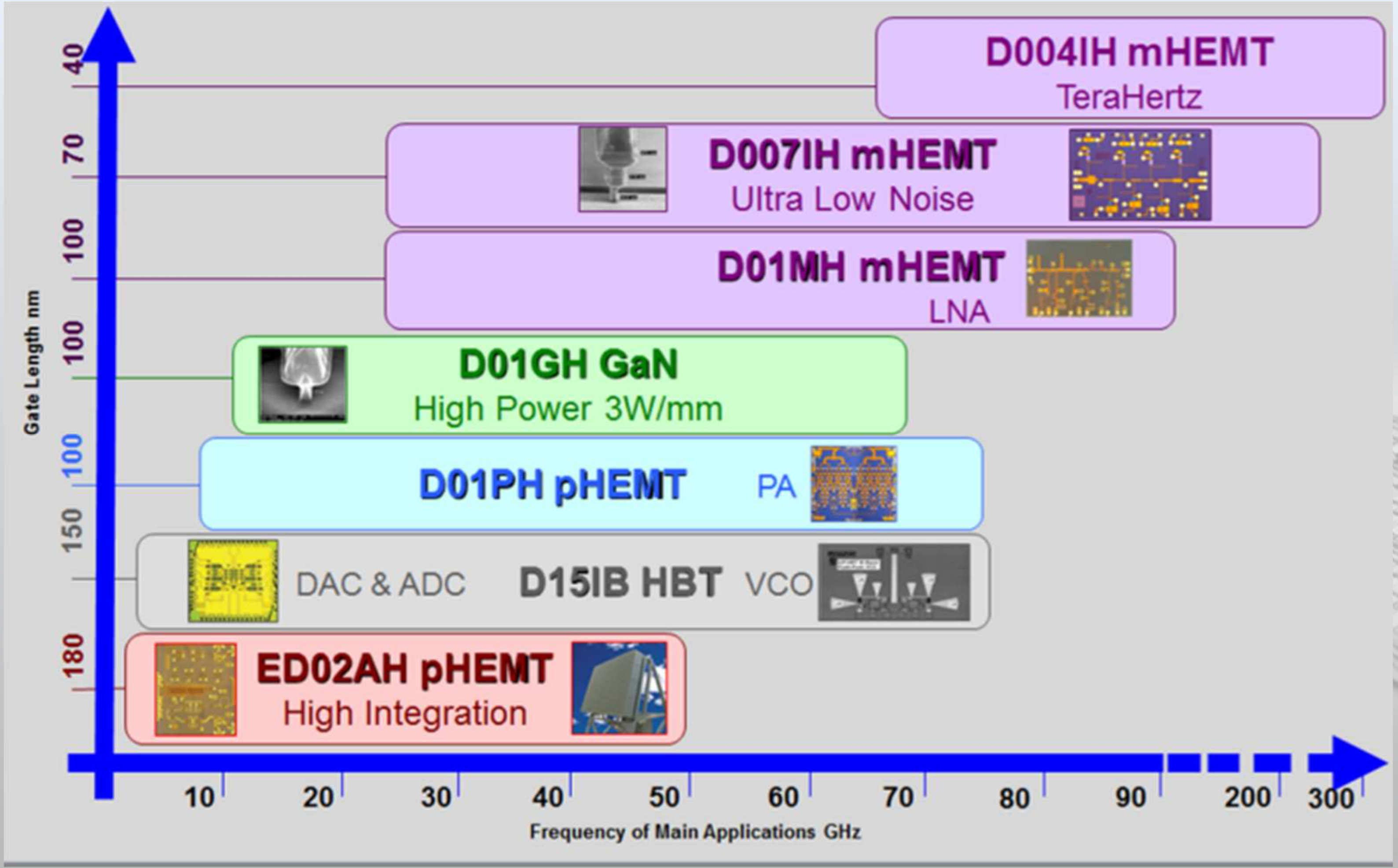
Microwave & RF

Europe's Independant IIIV Full-Service Foundry

Substrate → Epitaxy → Fab IC → Back-End → System

Epitaxy	Fab IC	Back-End
6-inch Epi Reactors	E-beam Lithography	RF On Wafer Test
	i-Line Steppers	Packaging
HBT & GaN	**Gate <40nm**	**Hi Rel**

OMMIC PROCESS



D004IH mHEMT
TeraHertz

D007IH mHEMT
Ultra Low Noise

D01MH mHEMT
LNA

D01GH GaN
High Power 3W/mm

D01PH pHEMT PA

DAC & ADC **D15IB HBT** VCO

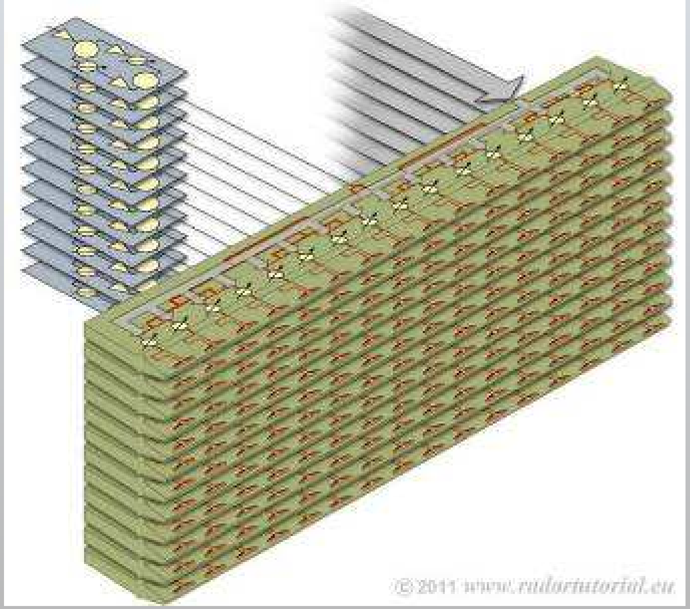
ED02AH pHEMT
High Integration

OMMIC ED02AH D/A mixed process for control functions

Introduction

- III/V provide optimum trade-offs in terms NF, gain, power and linearity for various applications including wireless telecommunication infrastructure, security scanners, radars and instrumentation.

- A weaker feature of III/V technologies → limited level of integration.



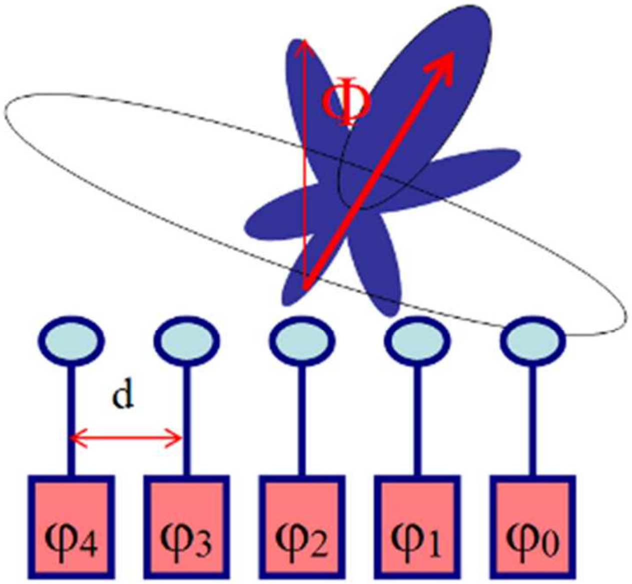
We will show how E/D PHEMT processes enable the integration of analogue functions like phase shifters and attenuators with serial to parallel converters

E/D → Serial ctrl → High integration → cost reduction

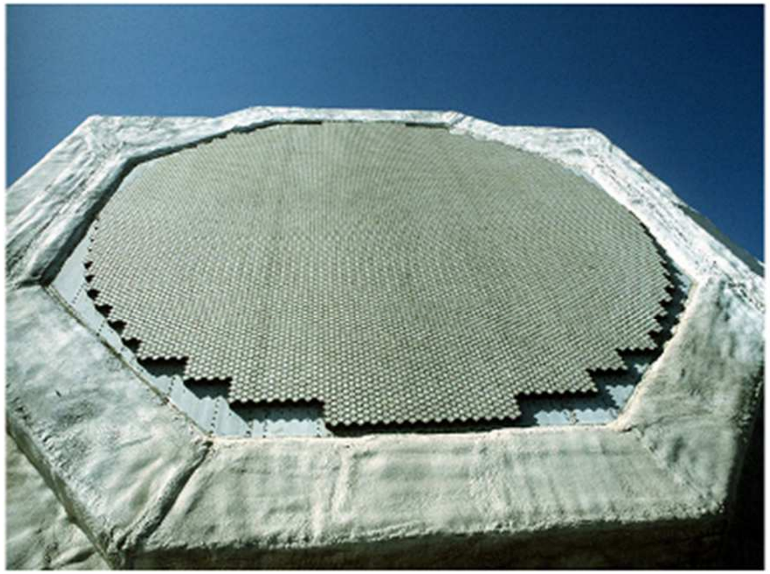
All integrated on the same chip to achieve state of the art performance through the example of Corechips.

Electonically steerable antenna example

The orientation of the beam is obtained by the use of variable phase shifters attached to each radiating element



$$\varphi_i = \varphi_0 + 2.i.\pi.d / \lambda \;.\; \sin(\Phi)$$



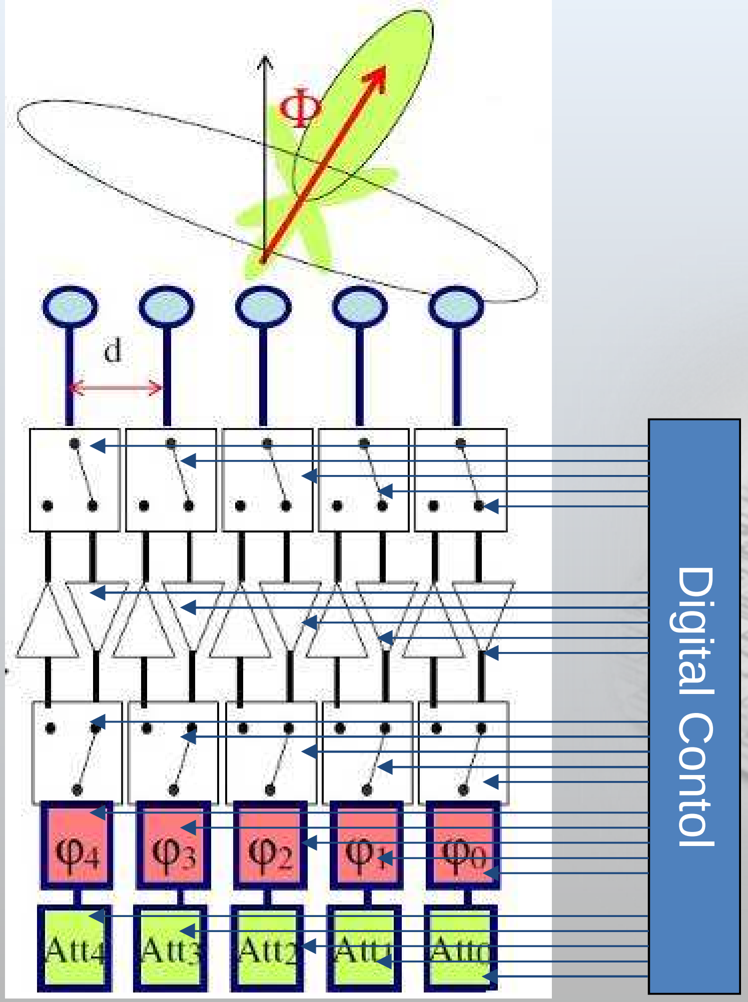
Source: U.S. Air Force/SSGT Lono Kollars

The side lobes may then be controlled by variable attenuators attached to each element

Electonically steerable antenna example

Each antenna element may contain :
- •A variable phase shifter
- •A variable attenuator
- •Switches, to be able to use the same system in receive or transmit modes
- •Amplifiers:

to compensate the losses and create some gain,
to reduce the noise in receive mode,
to create enough power to drive power amplifiers in transmit mode

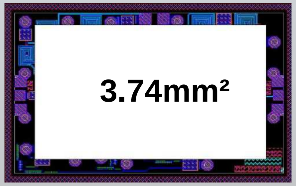


From single function to multiple function chip

Due to higher frequency of radar application , integration of functions become a key aspect of designs. *Below is the X band example*

Single functions already exists

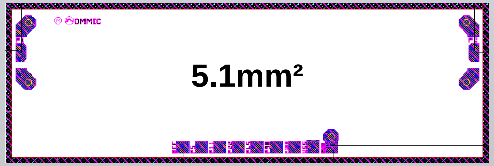
LNA



X band LNA

32dB gain 1.1dB NF

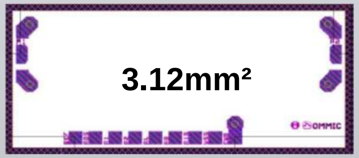
Dig Ph Shifters



X band Ph shifter

6 bit parallel control

Dig Attenuators



X band Attenuator

6 bit parallel control

MPA

X band MPA

23dBm Psat

Serial Interface need : 6 bit corechip example

With 12 bits (or more) for a full core chip, we are faced with a connection problem:

↓

Up to 24 pads (2 per bit if +/- control is required) to drive the 12 bits

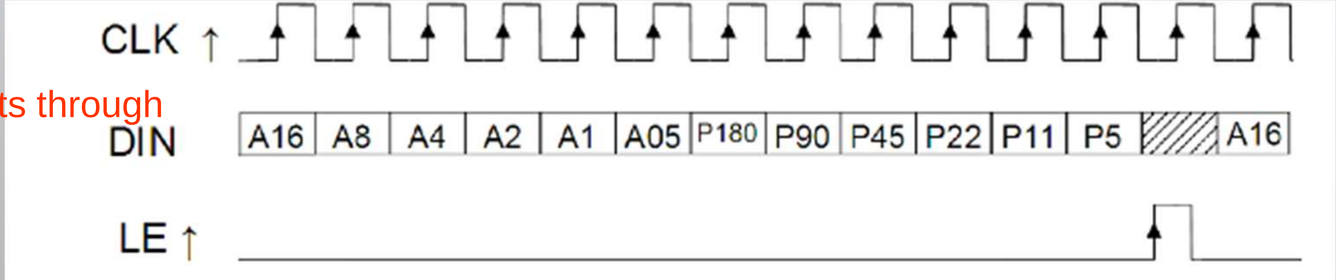
↓

24 bonding wires per circuit, multiplied by hundreds of
circuits

↓

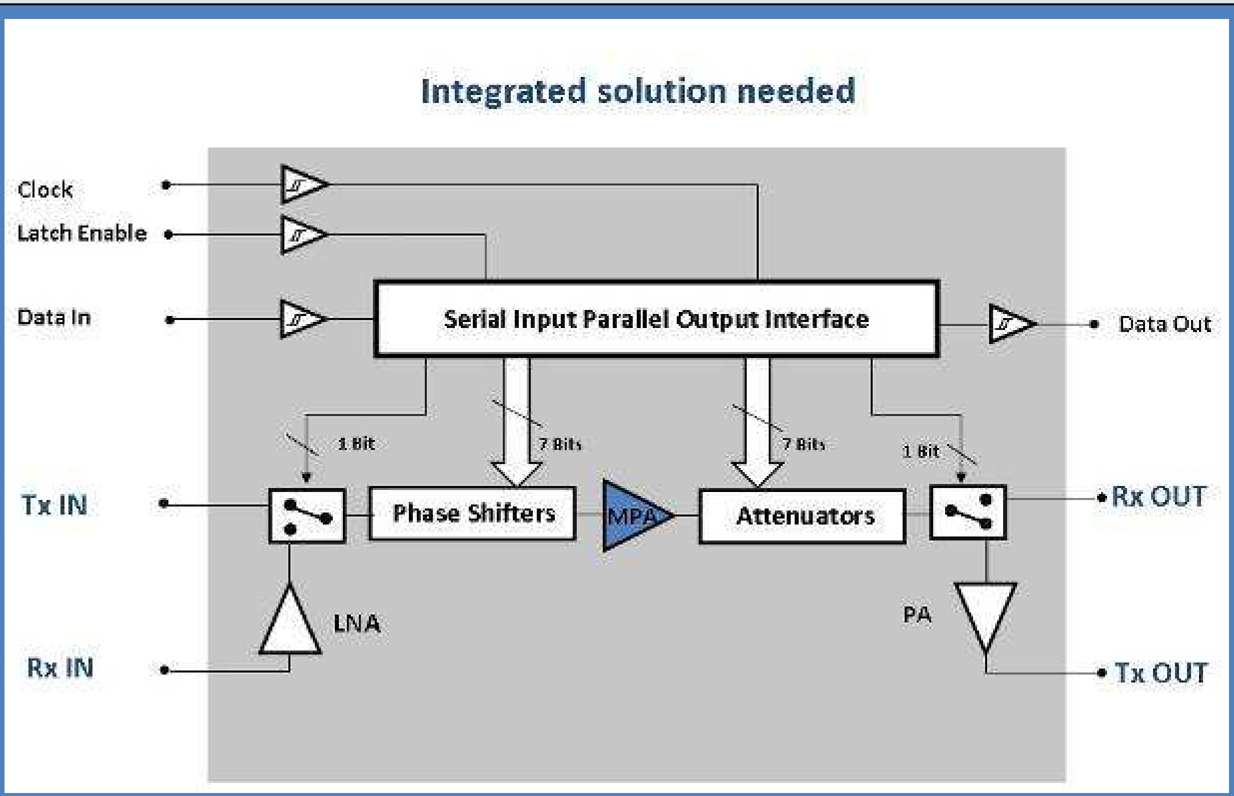
The solution is to place the SIPO on the chip

Only one PIN to control all bits through
Serial **I**nput **P**arallel **O**utput

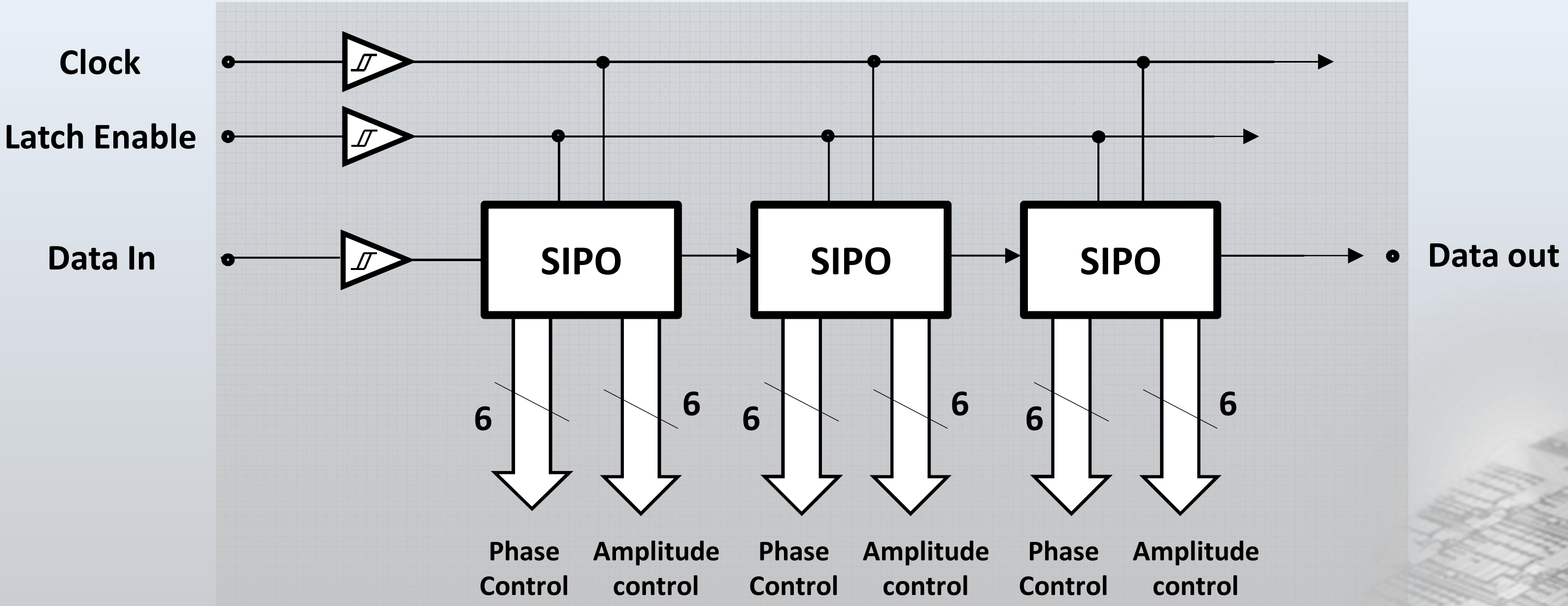


From single function to multiple function chip

Due to higher frequency of radar application , integration of functions become a key aspect of designs. *Below is the X band example*



Multiple Cascaded devices : The SIPO Advantage



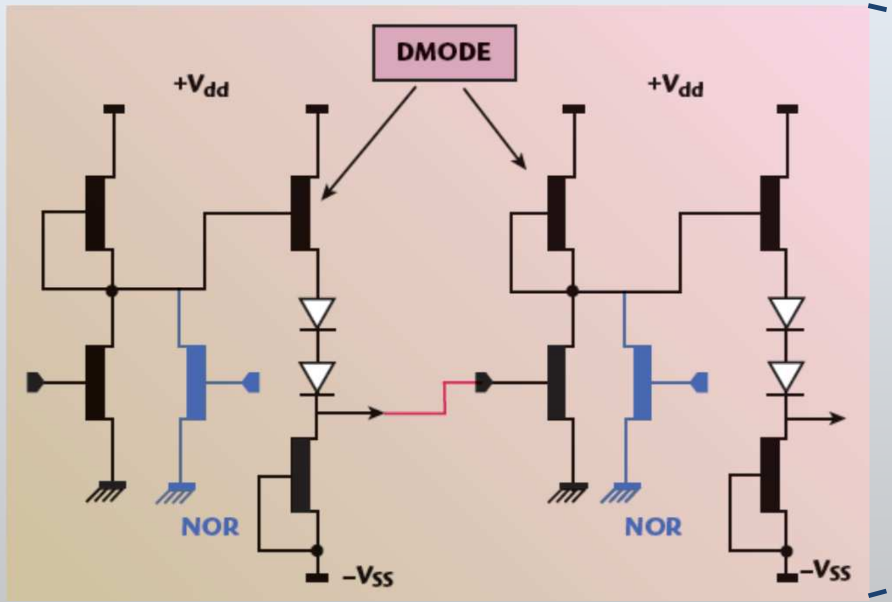
N devices to control :

2 x 6 x N wires for Parallel controled devices

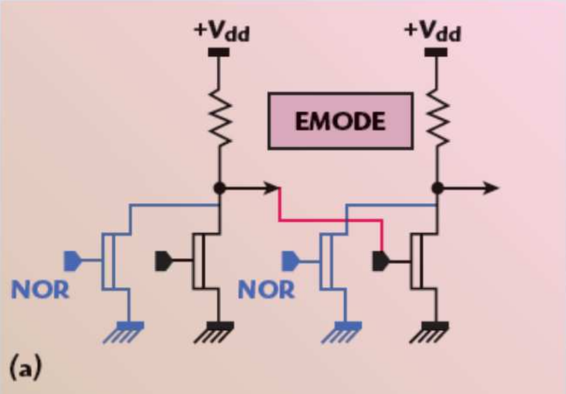
Only 3 wires for cascaded SIPO enabled devices

How to realize the SIPO

Efficient SIPO on chip requires Enhancement mode process

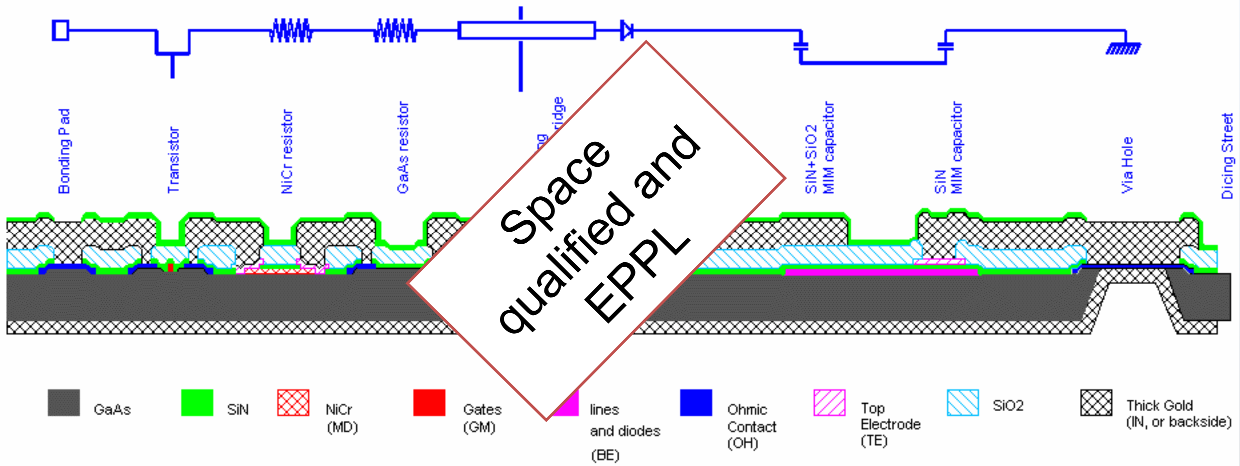


With D-mode transistors
Requires negative supply + DC level shifting

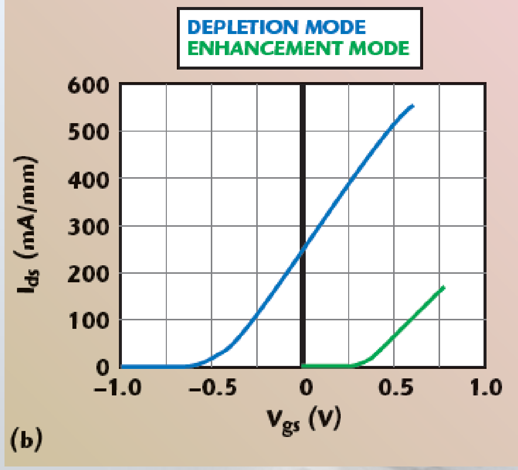


With E-mode transistors
Direct coupling

OMMIC E/D process : ED02AH

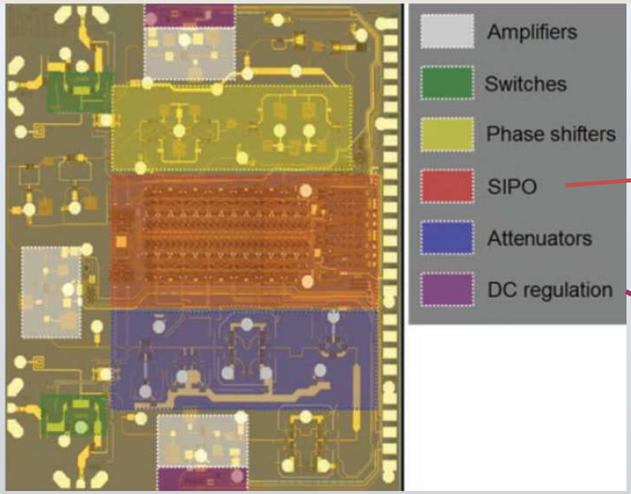


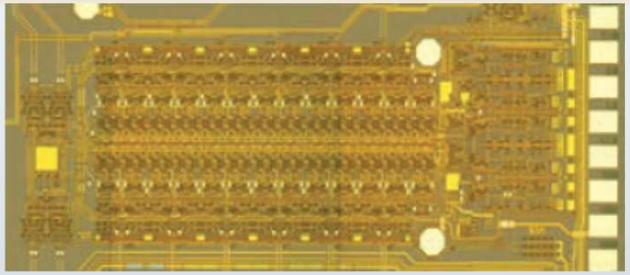
Space qualified and EPPL

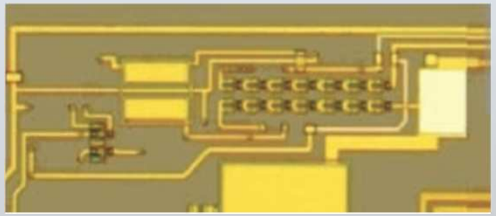


- Hetero-epitaxy with a pseudomorphic (GaInAs) active layer
- 0.18µm gate length (60 GHz Ft)
- Depletion and Enhancement mode recessed transistors: Vt=0.225V or -0.9V
- 2 types of diodes (0.18µm "GM" and 3µm "BE") for mixing, level shifting, or varactors.
- 3 types of Resistors : 40, 200 or 500 Ohms.square
- 2 types of MIM Capacitors : 50 or 400 pF/mm2
- Full SiN + SiO2 + SiN protection ensuring high reliability
- SiO2/SiN + air bridge isolation between layers to reduce the parasitic capacitances.
- 1.25µm or 2.5µm thick gold metallisation for interconnections and spiral inductors.
- Via holes through the 100µm substrate to reduce parasitic inductances to ground.

Examples of SIPOs





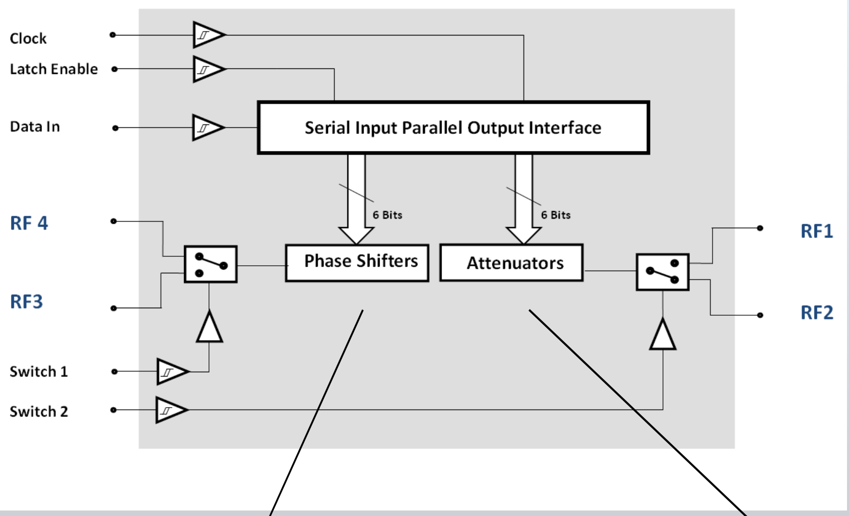


26 bits
SIPO

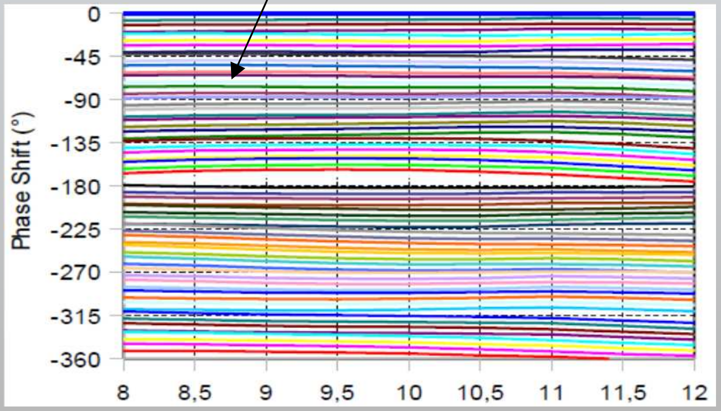
Number of control bits	Number of transistor gates	Global DC consumption including drivers and latches
12	700 (58 / bit)	150 mW (13 mW / bit)
26	1500 (58 / bit)	350 mW (13 mW / bit)
18	1500 (83 / bit)	300 mW (17 mW / bit)
24	1500 (63 / bit)	200 mW (8 mW / bit)
26	1200 (46 / bit)	60 mW (2.3 mW / bit)
10	800 (80 / bit)	4 mW (0.3 mW / bit) Low speed

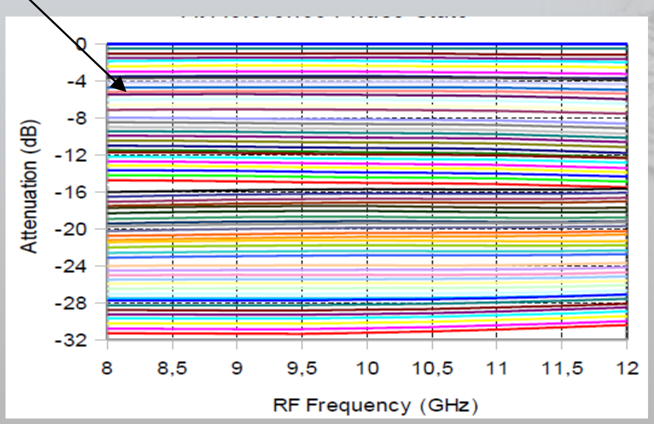
Examples of X band Corechips

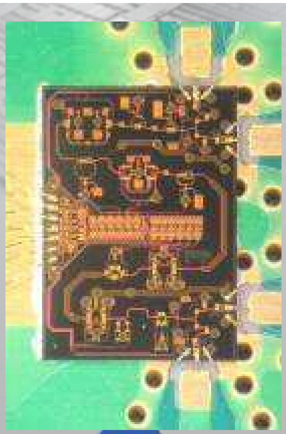
CGY2170XUH/C2 : 4 ports – 6bits
External LNA and PA



- Operating Range : 8 GHz to 12 GHz
- Insertion Loss : 15 dB @ 10 GHz
- RMS Phase Error ≈ 3.0° @ 10 GHz
- RMS Amplitude Error ≈ 0.3 dB @ 10 GHz
- Input P1dB ≈ +20 dBm
- S_{11} & S_{22} ≈ -15 dB @ 10 GHz (all states)
- Total Power Consumption ≈ 40 mW
- Chip size = 4000 x 2850 µm
- Tested, Inspected Known Good Die (KGD)
- Samples Available

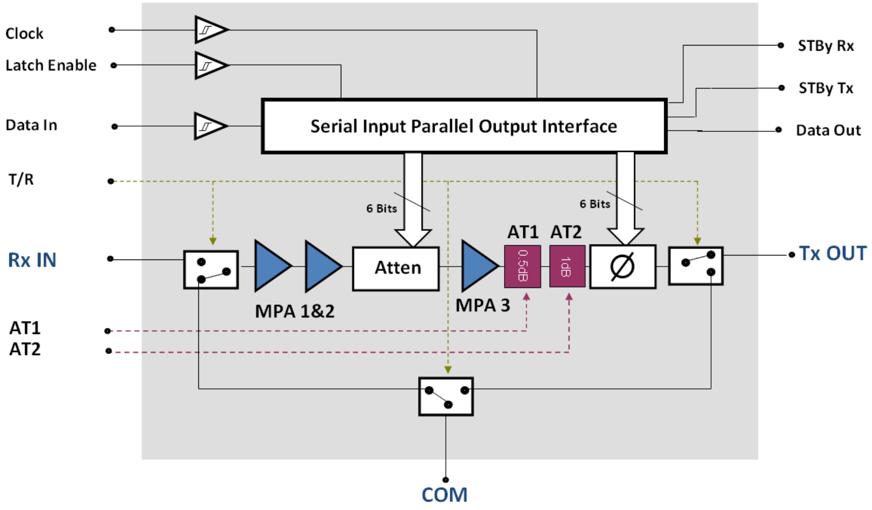






Examples of X band Corechips

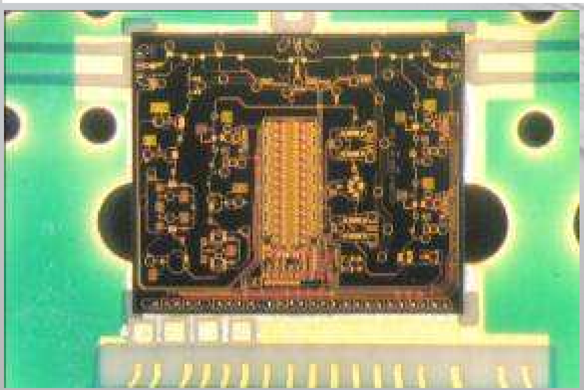
CGY2170YUH/C1 : 3 ports – 6bits
Internal MPA



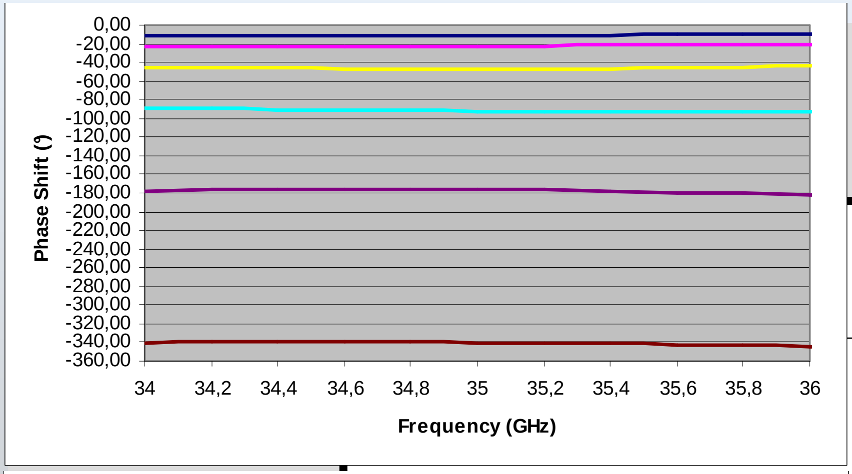
- Operating Range : 8 GHz to 12 GHz
- Gain Tx/Rx : 6 dB @ 10 GHz
- RMS Phase Error ≈ 3.0° at 9-10 GHz
- RMS Amplitude Error ≈ 0.4 dB from 8-11 GHz
- Output P1dB Tx ≈ +11 dBm
- Output P1dB Rx ≈ +11 dBm
- S_{11} & S_{22} < -17 dB @ 10 GHz (all states)
- Total Power Consumption ≈ 0,36 W
- Chip size = 4700 x 3800 µm
- Tested, Inspected Known Good Die (KGD)
- Samples Available

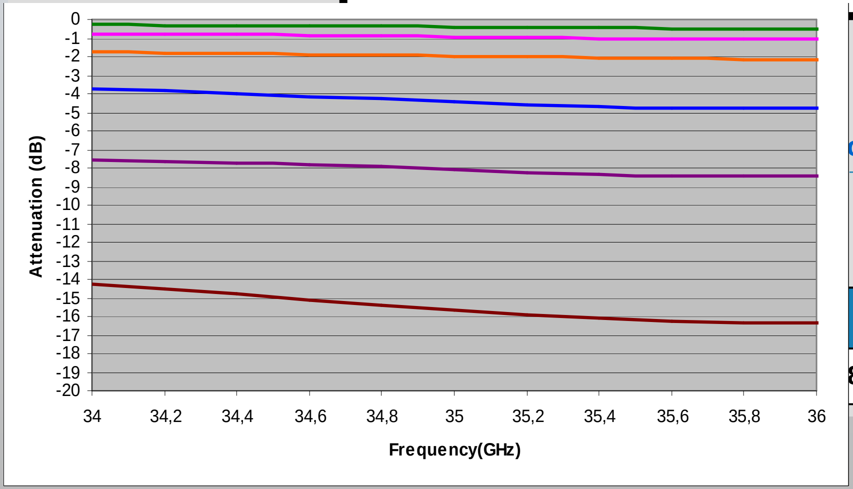
Separated register for Rx and Tx

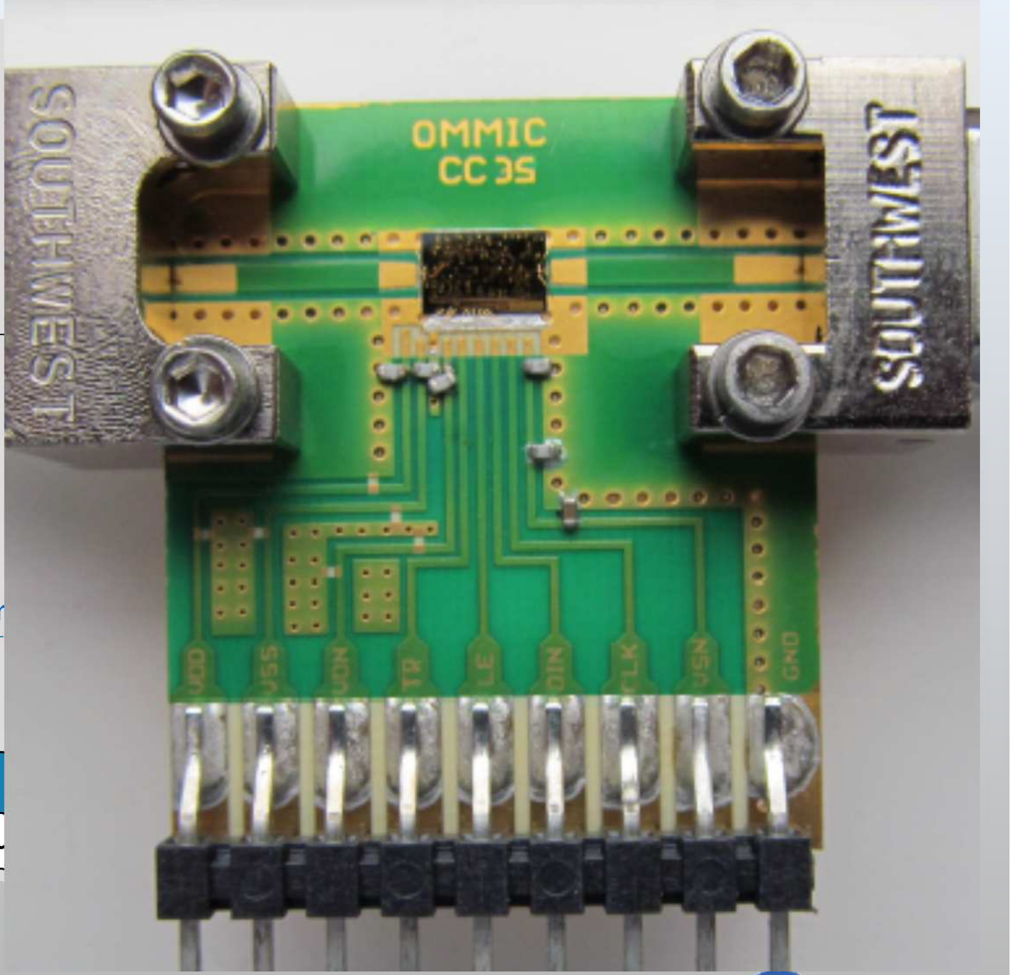
External additional attenuators



Nowadays brand new 35GHz Corechip

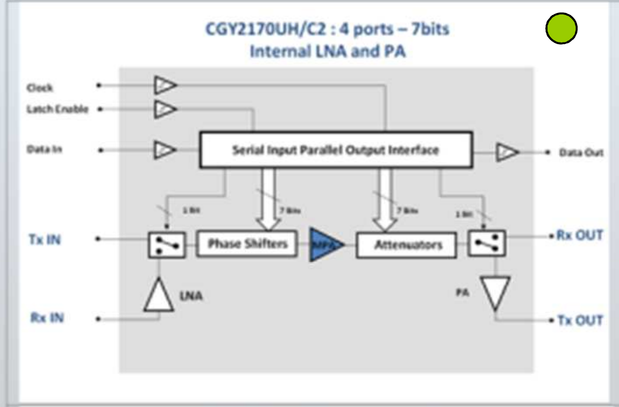




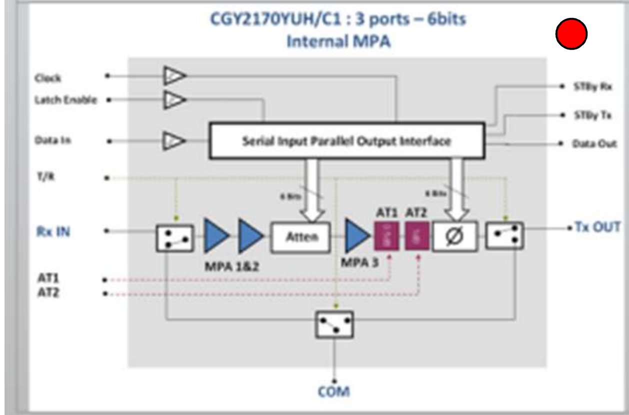


OMMIC Corechip offer

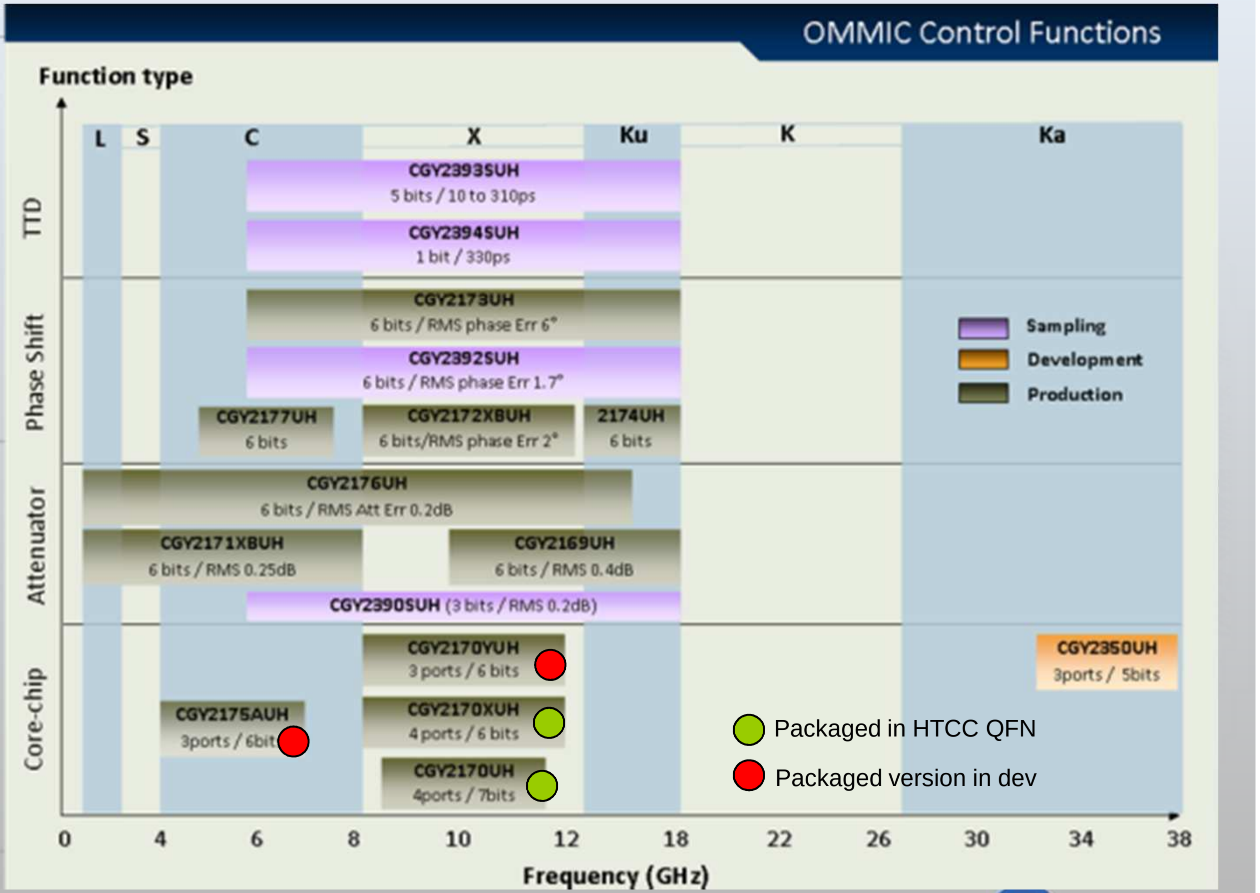
- **More than 15 Core chip in production from C band to Ka Band**
- **More than 40 Custom Corchip designed for customers**



CGY2170UH/C2 : 4 ports – 7bits
Internal LNA and PA



CGY2170YUH/C1 : 3 ports – 6bits
Internal MPA

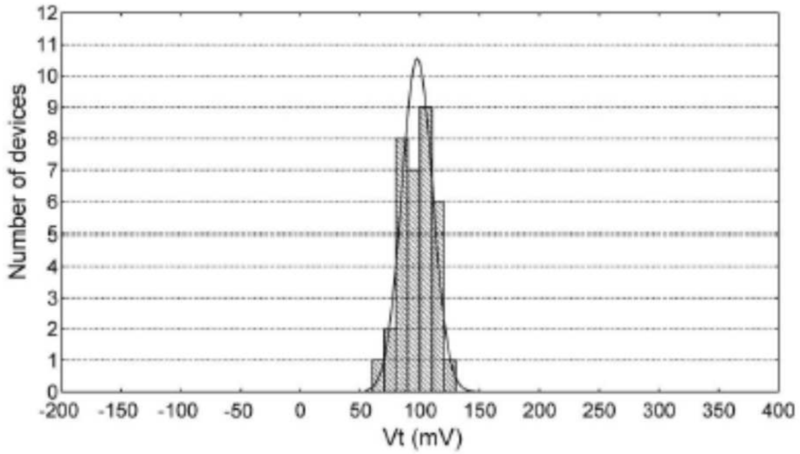


future control function

For the Development of Core Chips including SIPO above 60 GHz, a new process is required.

OMMIC has thus developed a true E-mode 0.1um process using a metamorphic layer

- 200 GHz Ft, 300 GHz Fmax
  - *=> E band Core Chip possible*
- 15 dB MSG @ 30 GHz
- E-mode => easy SIPO
- Large Vg swing => switches
- Same passives than ED02AH



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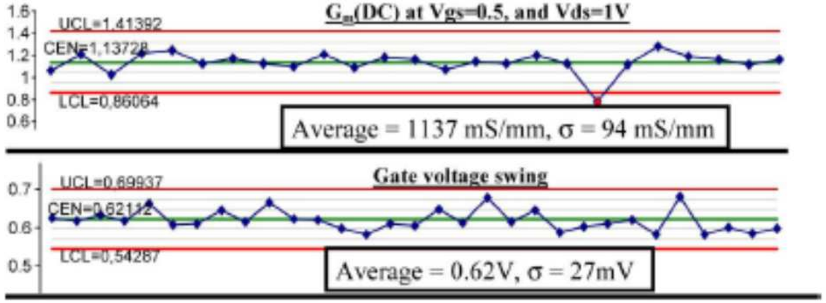


IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL. 54, NO. 7, JULY 2007, Hassan Maher (OMMIC) and Al

OMMIC GaN / Si

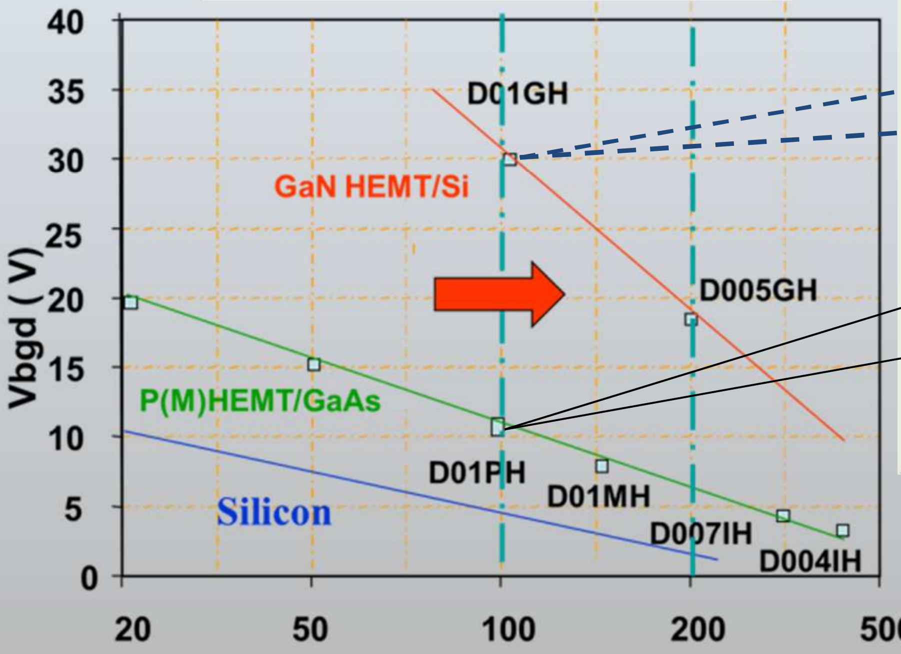
mmW GaN HEMT on Si : Goal

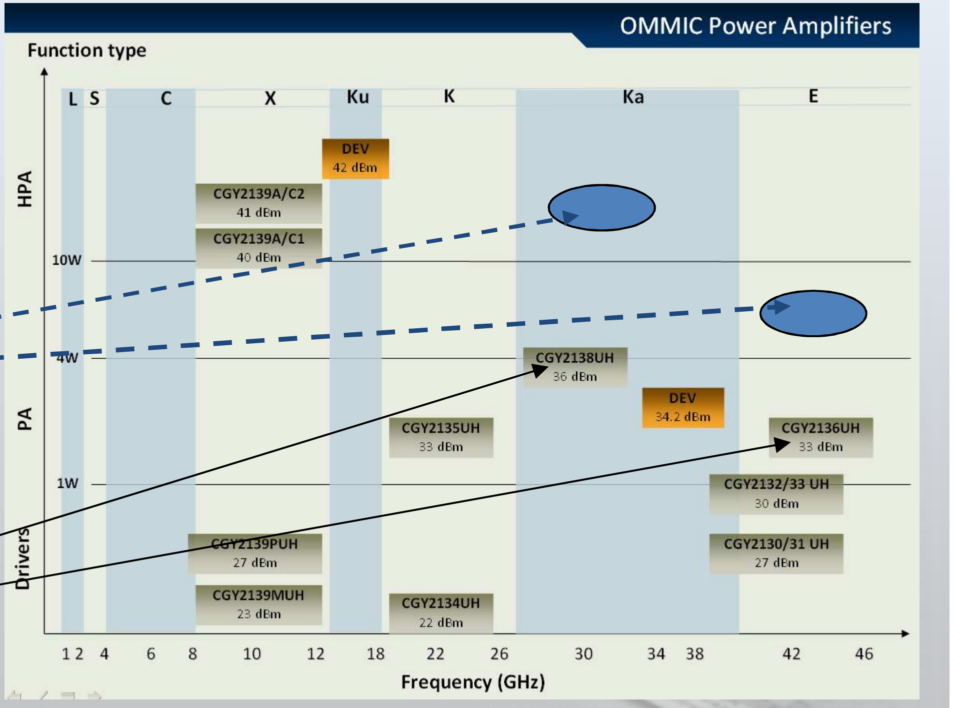
The choice of a GaN heterostructure on Si is dictated by the following points:

- Increase power density 3 times the current GaAs technology
- Address applications up to 20W, compatible with the Si Thermal conductance, primarily targeting frequency bands from 15 GHz and 100 GHz .
- Access to the epitaxial material without depending on SiC sources
- Full replacement of GaAs processes for professional applications up to 100GHz at a lower cost/mm2

mmW GaN HEMT on Si

- Idss (0V) = 650 mA/mm
- Vt= - 1.5V
- Gm max ext= 600 mS/mm
- Ft= 100 GHz, Fmax =180 GHz @ Vds = 3 V
- MSG = 14 dB @ 30 GHz
- Vbgd min =30V, typical = 40V (Vds max= 24V)
- Vdd =15V
- Psat> 2.5 W/mm at 30 GHz (Vds =15V)





Advanced release of GaN/Si process

Preliminary Design Kit available under ADS or AWR

D01GH :

- Idss (0V) = 650 mA/mm
- Vt= - 1.5V
- Gm max ext= 600 mS/mm
- Ft= 100 GHz, Fmax =180 GHz @ Vds = 3 V
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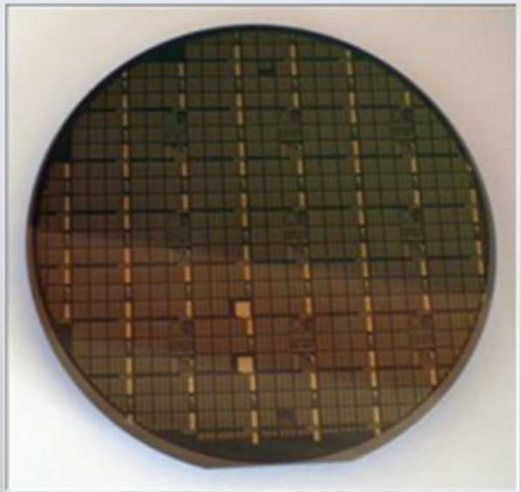
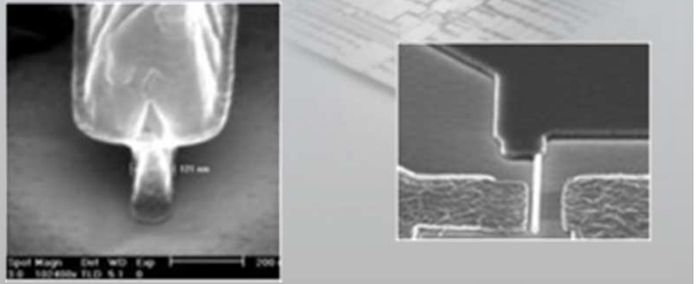


Applications :

- High frequency Power Amplifiers *10GHz to 94 GHz*
- Robust Low Noise Amplifiers (< 20 GHz)
- Robust Control Functions
- High Linearity Mixers

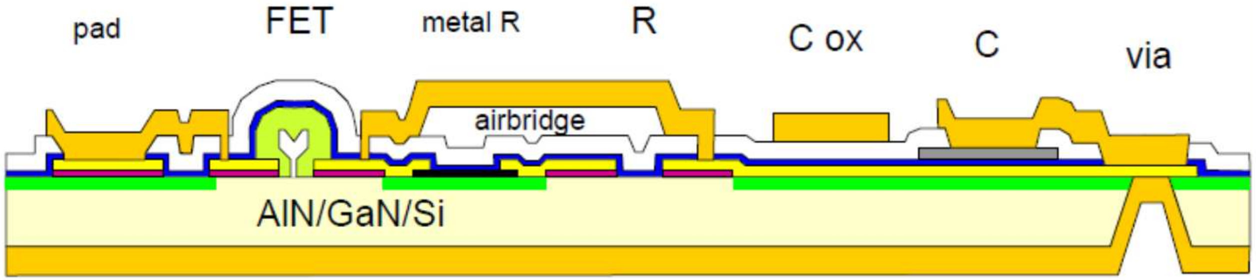


0.11 µm gate (GaN on Si)

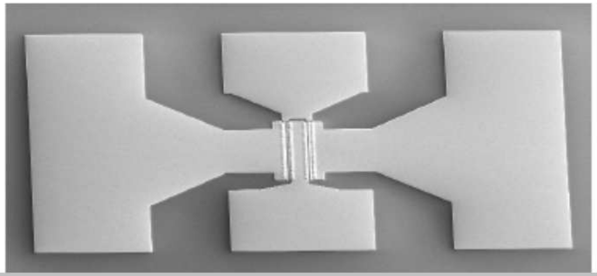
D01GH Key power applications and targets

- **Scaled GaN /Si (30% shorter gate) can replace GaAs and InP for power applications with following power capability :**
  - **1 W @ 94GHz**
  - **6 W @ 45GHz**
  - **12 W @ 30GHz**
  - **25 W @ 10GHz**
- **3 KEY features are required :**
  - **In situ SiN passivation (reduced lag effects in planar structure)**
  - **Si substrate with proprietary buffer and extension to 6 inch**
  - **Regrown ohmics (for high gm and low noise)**

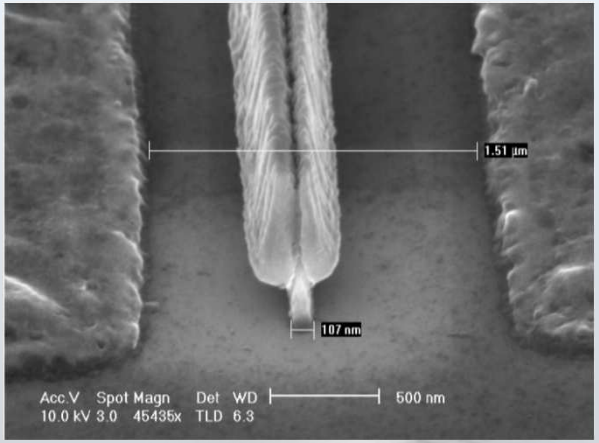
D01GH PROCESS FLOW

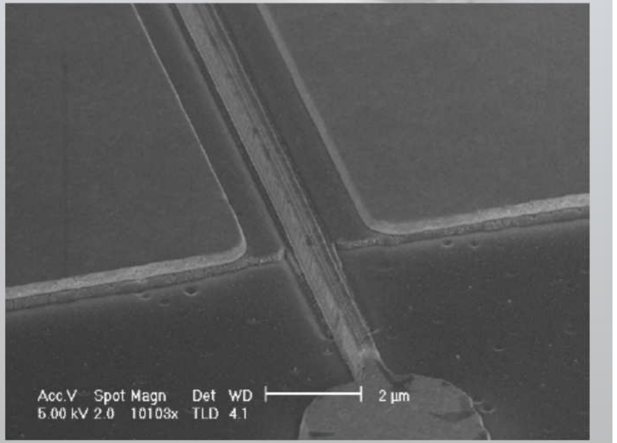


- •European epi (EPIGaN)
- •Regrown ohmics (for high gm)
- •Mushroom gate (100nm, 60nm)
- •In situ SiN passivation (for low lag effects <10%)



2x70um HEMT





Thank you for your attention

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