Fabrication de MMIC Intégrant des MEMS RF

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Plan

- OMMIC technologies
- Development of MEMS at OMMIC
- MEM-4-MMIC European FP7 project
  - MEMS circuit applications
  - RF-MEMS switch process
  - 0-Level/1-Level Packaging
  - RF-MEMS switch circuit performances
  - Application demonstrator
- Conclusion
OMMIC has a wide range of Technologies based around GaAs substrates:

- PHEMT - ED02AH Mixed Mode 60 GHz ft
- PHEMT - D01PH Power/Low Noise 105 GHz ft
- MHEMT - D01MH Low Noise 150 GHz ft
- MHEMT - D007IH Low Noise 300 GHz ft
- MHEMT - D004IH Low Noise 600 GHz ft
- HBT on InP - DH15IB Numeric 200GHz ft
- HBT on InP - DH05IB Numeric 300GHz ft
- GaN on Si - D01GH Power 90 GHz ft

- Applications are either civil, space and military
  - Ultra Low Noise Amplifiers for Base Stations
  - Control Functions for Phase Array Systems
  - Point to Point Links
  - Fiber Optic Interfacing
  - Passive Millimeter wave Imaging (Security etc)

**RF-MEMS development objective for OMMIC:**
Introduction a Commercial RF MEMS technology based around a SPST Device **Integrated with standard OMMIC MMIC Processes** with modeling and support.
RF-MEMS concept evolution

Standard unitary RF-MEMS

FlexMEMS (SEM view) to optimize activation voltage and to limit double transitions

RF-MEMS with multi-contact (to reduce contact resistance) and HF circuit
• In the "up" position, the designed height of the MEMS cantilever above the pull down electrode is 4 µm, and the distance between contacts is 2 µm.

• In the "down" position, a slight bow of the MEMS cantilever may make the height above the pull down pad too small, and the cantilever is pulled down on the dielectric covering the pull down pad, giving time dependent hysteresis by dielectric charging.

• The stiction is reduced by the introduction of a wedge (extra bar), with the same construction as the contacts.
<table>
<thead>
<tr>
<th></th>
<th>MEMS-4-MMIC (FP7 ICT STREP) 2008-2012</th>
<th>NANOTEC (FP7 ICT IP) 2011-</th>
</tr>
</thead>
<tbody>
<tr>
<td>Companies</td>
<td>IMST/Saab</td>
<td>Alfa Imaging</td>
</tr>
<tr>
<td>Applications</td>
<td>Sat.com/radar</td>
<td>passive imaging</td>
</tr>
<tr>
<td>Frequency</td>
<td>24 GHz / 35 GHz</td>
<td>94 GHz</td>
</tr>
<tr>
<td>Power handling</td>
<td>Low-power</td>
<td>Low-power</td>
</tr>
<tr>
<td>Noise figure</td>
<td>-</td>
<td>NF=2-4 dB (LNA)</td>
</tr>
<tr>
<td>Technology</td>
<td>150 nm (D01PH)</td>
<td>70 nm (D007IH)</td>
</tr>
<tr>
<td>Substrates</td>
<td>100 µm</td>
<td>200/600 µm</td>
</tr>
<tr>
<td>Backside process</td>
<td>µStrip</td>
<td>CPW</td>
</tr>
<tr>
<td>Basckside MEMS</td>
<td>Single chip protection</td>
<td>All wafer protection</td>
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<tr>
<td>protection</td>
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• RF MEMS offers several attractive properties (such as low losses and DC power dissipation, high isolation and linearity) that potentially can make it an enabling technology for wide-band (or multi-band) reconfigurable RF systems in future radar and wireless applications

• Reconfigurable RF MEMS based switching, matching, filtering and phase shifting circuits may be used in adaptive front-ends (for space, aerospace, security, defense & wireless communication)
Key areas of work
Noise-free SAR image. Speckle in the image present due to terrain roughness

SAR image for COTS (3 bit). Practically unusable

SAR image for RF-MEMS (3 bit). Much of the image information retained

Estimated SNR values

<table>
<thead>
<tr>
<th></th>
<th>Co-polar (HH)</th>
<th>Cross-polar (HV)</th>
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<tbody>
<tr>
<td>COTS 3-bit</td>
<td>6.6 dB</td>
<td>-2.2 dB</td>
</tr>
<tr>
<td>COTS 5-bit</td>
<td>1.6 dB</td>
<td>-7.2 dB</td>
</tr>
<tr>
<td>RF-MEMS 3-bit</td>
<td>11.6 dB</td>
<td>2.8 dB</td>
</tr>
<tr>
<td>RF-MEMS 5-bit</td>
<td>8.6 dB</td>
<td>-0.2 dB</td>
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</tbody>
</table>

SAR image simulation results: Impact of phase shifter performances

MEMS4MMIC European FP7 Project
MEMS4MMIC project framework

- IMST (Leader & Antenna) Germany
- OMMIC (Process & Reliability) France
- FOI (Architecture & Design) Sweden
- VTT (LTCC packaging & Design) Finland
- SAAB (Design) Sweden
- IEMN (Packaging) France
- IMT (Antenna) Romania

Site web: www.mems4mmic.com
- The D01PH process is a power process for applications up to 50 GHz, with very low noise.
- E-beam written mushroom gate with $L_g = 135$ nm.
- $F_t = 100$ GHz
- $B_{gd} = 9$ V (min) 11V (typ)
- $V_{ds\ max} = 7$ V (min) 8 V (typ)
- $I_{max} = 700$ mA/mm
- $F_{min} = 0.5$ dB @ 12 GHz
RF-MEMS Process Development

GaAs Substrate

MEMS features at the end of Standard front-end process

Deposition of seed layer and cantilever definition

Contact and wedge plots deposition

Deposition of cantilever metals

Deposition of sacrificial layer and pillars definition

Photoresist and seed layer removal
RF-MEMS Process Development

All-wafer MEMS protection for back-end processing

- GaAs Substrate
- MEMS before back-end process
- CPW back-end process
- GaAs Substrate 200µm
- MEMS liberation
- GaAs Substrate 200µm
- Specific MEMS protective layer deposition

Type of photoresist, thickness and baking conditions carefully optimized for cleaness of release
We introduce the MEMS contact switch

This switch must have low contact resistance (high contact force), yet be small enough for mm-wave use (~200 µm) hence high actuation voltage. The actuation voltage must not influence the MMIC circuit, hence no direct contact between actuation circuit and semiconductor material! This has been achieved in the process integration.

The MEMS must support the backside process, during which the wafer is glued with the frontside to a sapphire carrier wafer. Release of the wafer from the carrier (24 h solvent !) should not release the MEMS → protection step necessary.

Wafers cannot be diced after MEMS release!!
The next step is to protect the front-end of the future dies individually, to protect it during wafer thinning and backside process.

PECVD (SiN) deposition at 100°C for MEMS protection during back-end process.

Removal of protective SiN layer and MEMS release.

The next step is the backside process including RIE (chloride), metal sputtering and electrolytic gold deposition.

Need to put wafer on 4” carrier wafer before the MEMS release to be able to do the bonding step of the 0-level packaging, due to fragility of 100µm wafers.
The final process flow was introduced in OMMIC process and wafer management software.
Specific procedures for MEMS realization have been drafted.
0-Level packaging (BCB)

Integration with IEMN 0-Level packaging process

100µm thin wafer with via-holes with RF MEMS released

Deposition of BCB cap

Additional SiN protection and contact opening
Improvement of BCB cap process:

- Partial BCB dry etching is used to achieve flat BCB sealing ring, which is very important for a better BCB bonding.
The BCB cap has been patterned on Si wafer covered with an anti-adhesion layer called “monolayer”.

The Sealing of the cap on the final thinned to 100µm circuit wafer is realized by thermo-compression.

For the sealing operation, the 100µm thin circuit wafer, which is too fragile, is glued to a thick 4” carrier wafer.
0-Level packaging (BCB)

Example of 0-Level packaged circuits
Development of low-temperature soldering process:

- Earlier used AuSn requires >320 C processing temperature

- Hermetic packages with SnBiAg solder (soldering T=175 C)
Individual RF-MEMS (FOI measurements)

- Insertion loss @ 40GHz around 1dB
- Isolation @ 40GHz close typically to 19dB
- Resonance at 34GHz, 62GHz and 96GHz is due to the to close line of the shunt RF-MEMS below
Individual RF-MEMS (VTT measurements)

Additional measurement realized on a different circuit (without shunt RF-MEMS) shows similar results without the resonances.

Those additional measurements have been performed on 0-level packaged devices and demonstrate the absence of negative impact of BCB capping on RF performances.
Measurement results of 11 SPST switches on VTT7 circuit

The switch performances is relatively good up to 60 GHz:
- isolation > ~30 dB
- return loss > ~15 dB
- insertion loss < ~2.5 dB

Agreement between the measured and the Sonnet EM simulation data is rather good at the whole frequency band till 110 GHz.
SP4T (Single Pole 4 Throw) circuit design by IMST allowed to choose from 4 inputs using 2 rows of RF-MEMS to switch the signal.

Insertion loss: (2 serial RF-MEMS switch) below 2dB up to 65GHz
Return loss: below -15dB on the overall bandwidth
Isolation: around 35dB at 24GHz and above 20db up to 65GHz.
GaAs RF-MEMS based active MMICs
FOI/IMST co-designed SP4T switched LNA
(chip dimensions equal 1.5 mm x 2.0 mm)

Measured s-parameters of a wideband GaAs RF-MEMS based SP4T switch circuit (IMST design): ON/OFF state transmission ($s_{21}$) when the switches used in each of the four branches have been switched on/off, respectively (shown to the left and right, respectively)
GaAs RF-MEMS based active MMICs
FOI/IMST co-designed SP4T switched LNA
(chip dimensions equal 1.5 mm x 2.0 mm)

Measured s-parameters of a wideband GaAs RF-MEMS SP4T switched LNA circuit with 17-18 dB of maximum gain and 20-30 dB of switched in-band isolation
GaAs RF-MEMS based active MMICs
FOI/IMST co-designed SP4T switched LNA
(chip dimensions equal 1.5 mm x 2.0 mm)

- Measured noise figure of a GaAs MEMS SP4T switched LNA MMIC is around 3 dB at 15-25 GHz
- NF ≥ 2.7 dB at 20 GHz which is 0.6 dB higher than the simulated noise figure value of the fixed LNA design
- The relatively small impairment in switched LNA gain and NF is due to the on-chip wideband MEMS SP4T switch used within this design with a loss of about 0.7 dB at 20 GHz.
Application demonstrator

Steered beams antennas
Application demonstrator

Steered beams antennas

Simulated beams at 24GHz

Measured beams at 24GHz

Assembled and measured by IMST
• Successful integration of cantilever contact switch MEMS into OMMICs standard MMIC processes, with 0.5 dB insertion loss @ 30 GHz and 1.5 dB @ 94 GHz.

• Technological solutions have been found to improve switching performances and yield

• A complete process, including back-end and 0-level packaging, is now well defined with the corresponding design rules (not transferred from IEMN)

• Functioning circuits with 0-level packaging have been produced and tested
### RF-MEMS Process Development

#### 3 RUN were made during the MEMS4MMIC project:

<table>
<thead>
<tr>
<th>Mask</th>
<th>Batch</th>
<th>Purpose</th>
</tr>
</thead>
<tbody>
<tr>
<td>MEMSESA01</td>
<td>6557, 6563, 6587, 6624, 6742, 6820, 6821, 6886</td>
<td>MEMS evaluation, and process stabilization&lt;br&gt;Introduction of FLEXMEMS design&lt;br&gt;MEMS only circuits</td>
</tr>
<tr>
<td>M4M2010</td>
<td>7003, 7004, 7007, 7188, 7214, 7215, 7231, 7232, 7454, 7510</td>
<td>Active devices and MEMS all-together circuits&lt;br&gt;Introduction of back-end process</td>
</tr>
<tr>
<td>M4M2011</td>
<td>7659, 7668, 7670, 7675, 7697, 7700</td>
<td>Final circuits for demonstrators&lt;br&gt;Introduction of wedge and BCB capping IEMN technology</td>
</tr>
</tbody>
</table>
Integration with IEMN 0-Level packaging process

100µm thinned wafer glued on support wafer using thermo-compression technique
Integration with IEMN 0-Level packaging process

Problem of yield after the back-end process due to porosity of SiN protection layer (separation from sapphire support to be optimized)

We limited this problem by separating the protective resist layer between the chips with a special lithography step, before putting the SiN protection layer (Otherwise, a single hole destroys the whole wafer !!)

100µm thinned wafer after back-end processing with substrate vias, and before RF-MEMS release
GaAs RF-MEMS based active MMICs
FOI/IMST co-designed wideband Dicke switched LNA
(chip dimensions 1.5 mm x 2.0 mm)

Measured s-parameters of three characterized wideband GaAs RF-MEMS based
Dicke switch circuits (FOI design): ON state transmission and OFF-state
isolation (upper left), ON state transmission (upper right) and ON state input
matching (lower left)
GaAs RF-MEMS based active MMICs
FOI/IMST co-designed wideband Dicke switched LNA
(chip dimensions 1.5 mm x 2.0 mm)

Measured s-parameters of five characterized wideband (16-37 GHz) GaAs RF-MEMS based (Dicke) switched LNA circuits with about 17 dB of maximum gain and around 20 dB of switched isolation at 5-40 GHz.
- The measured noise figure of a GaAs MEMS (Dicke) switched LNA MMIC is around 3 dB at 15-25 GHz.
- The noise is equal to 2.8 dB at 20 GHz (which is 0.7 dB higher than the simulated noise figure value of the fixed LNA design).
- The relatively small impairment in switched LNA gain and NF is due to the on-chip wideband MEMS (Dicke) switch used within this design with a loss of around 0.6 dB at 20 GHz.
Activation cycling for **uncapped** RF-MEMS:
- Erratic activation from time to time
- Contact resistance have **strong** variation during lifetime
- RF-MEMS stop activating after **several 1,000** of activations

Activation cycling for **capped** RF-MEMS:
- Erratic activation from time to time
- Contact resistance have **very limited** variation during lifetime
- RF-MEMS can still be activated after **several 100,000** of cycles

The comparison between 3Hz and 100Hz activation cycling indicates a dependence of lifetime with the activation frequency.