Le salon des radiofréquences, des hyperfréquences, du wireless, de la CEM et de la fibre optique
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Potentialités et Applications de la filière GaN

What possible future for GaN on silicon substrate for power applications in microwave and millimeter wave?

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Outline

I. Motivations

II. Potential and applications of GaN

III. Substrates for GaN growth

IV. Technological process

V. Thermal management

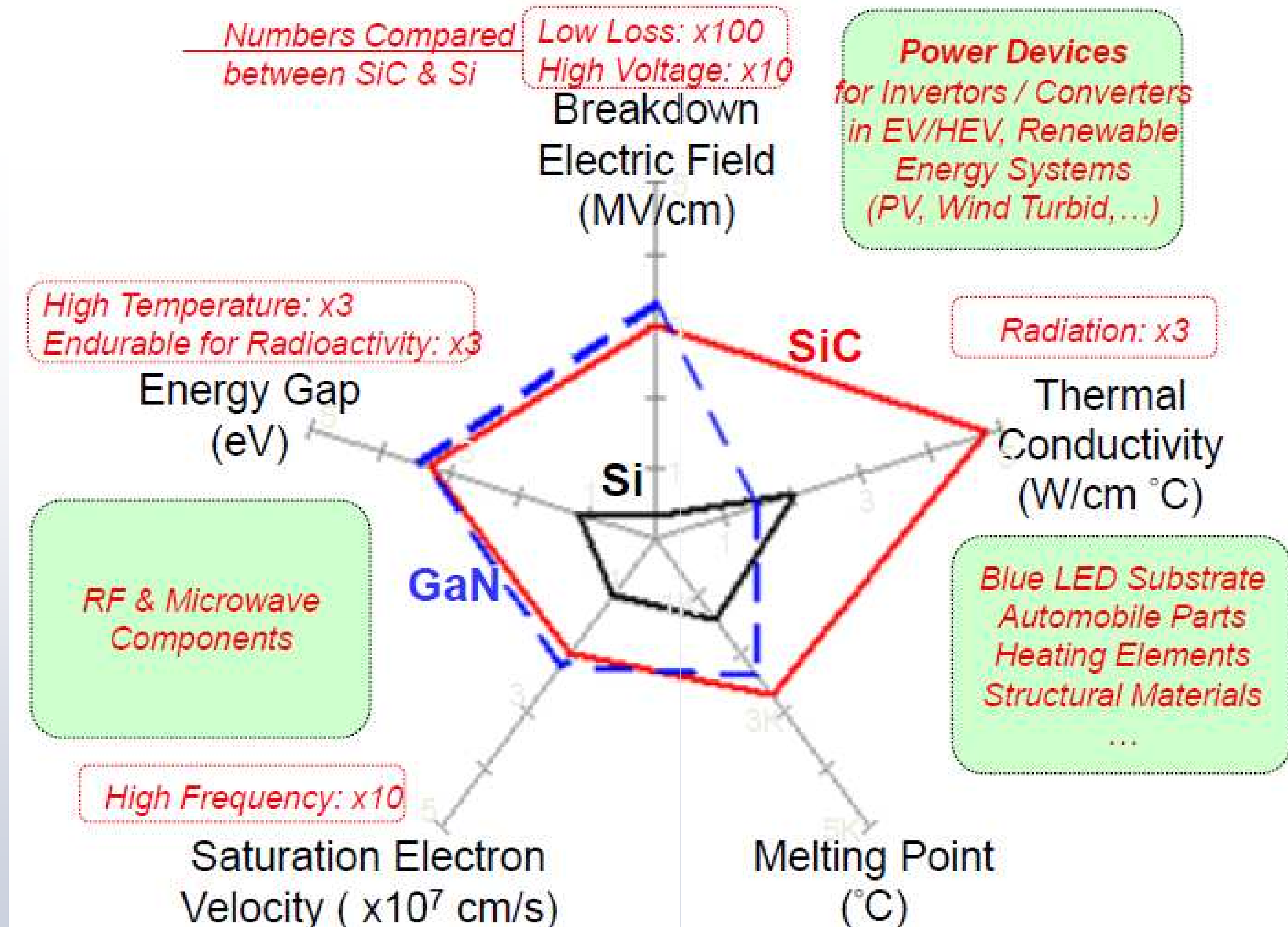
VI. Comparison of AlGaN/GaN heterostructure on Si substrate

VII. β-SiC/Si : 3rd possible way

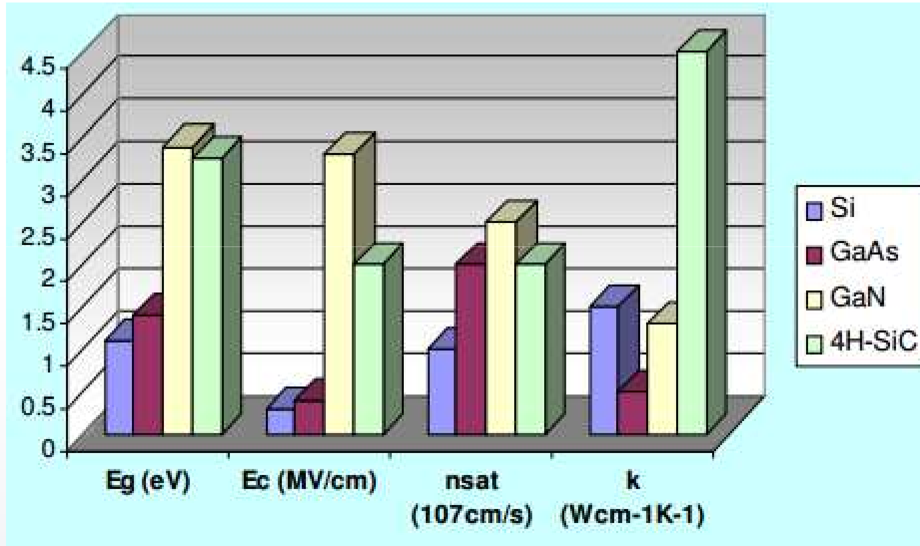
VIII. Example of some devices

IX. Some remarks and discussion

Comparison of WBGM properties for electronic

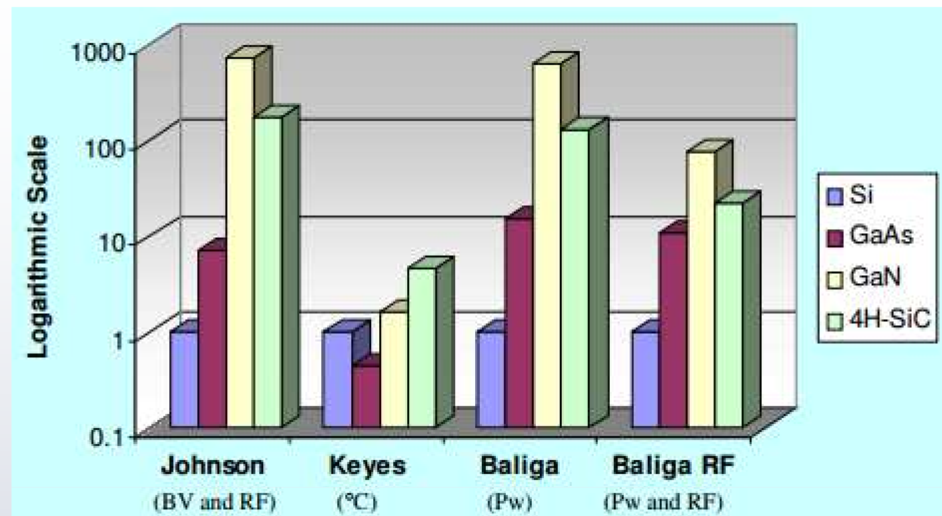


II. Potential & applications of GaN



Physical properties

Figures of merit



$$\mathrm{KMS} = \lambda\left(\frac{C \times V_{sat}}{4 \times \pi \times \varepsilon}\right)$$

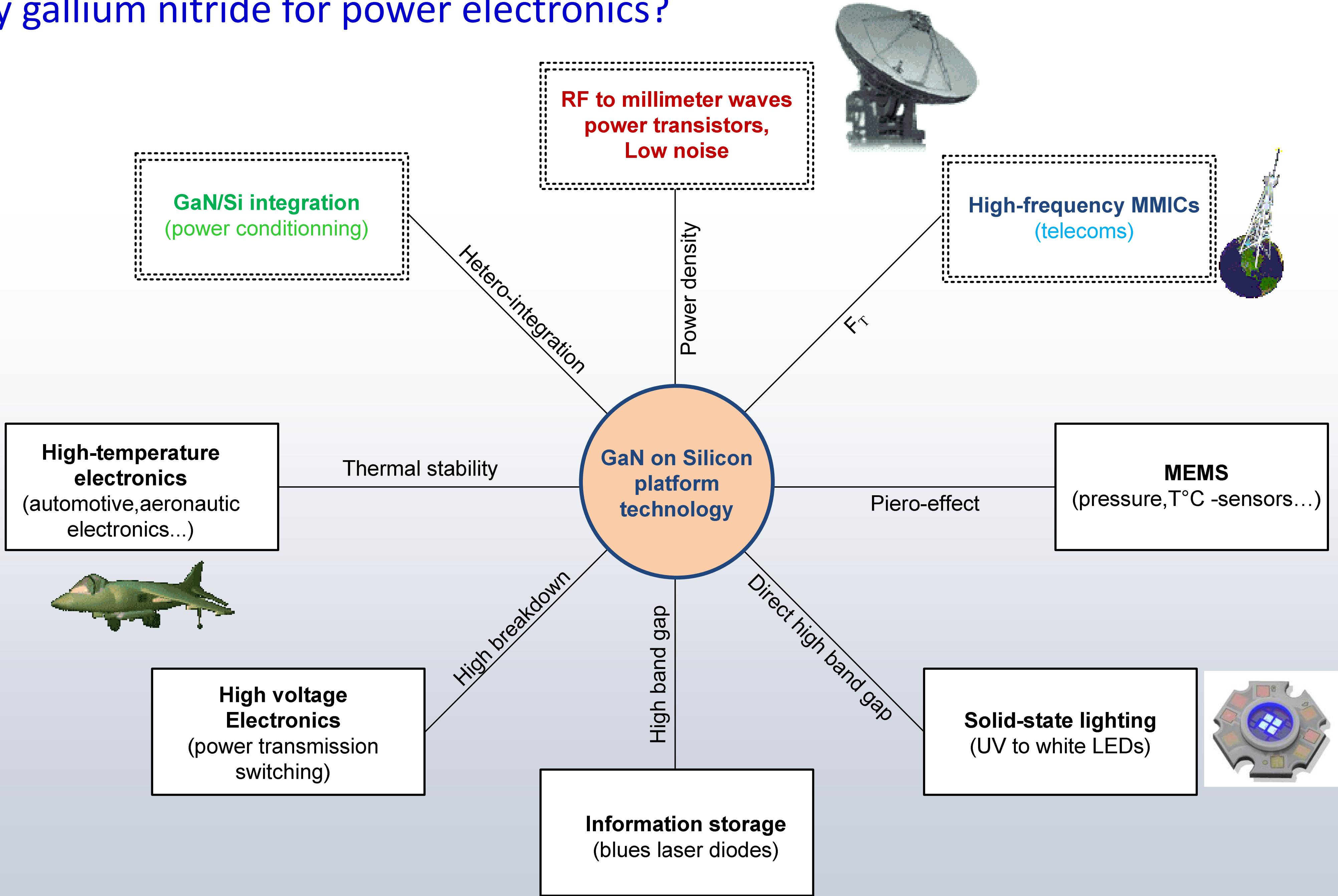
$$\mathrm{BFM} = \varepsilon \times \mu \times E_c^3$$

12 (bulk)
26 (hetero)

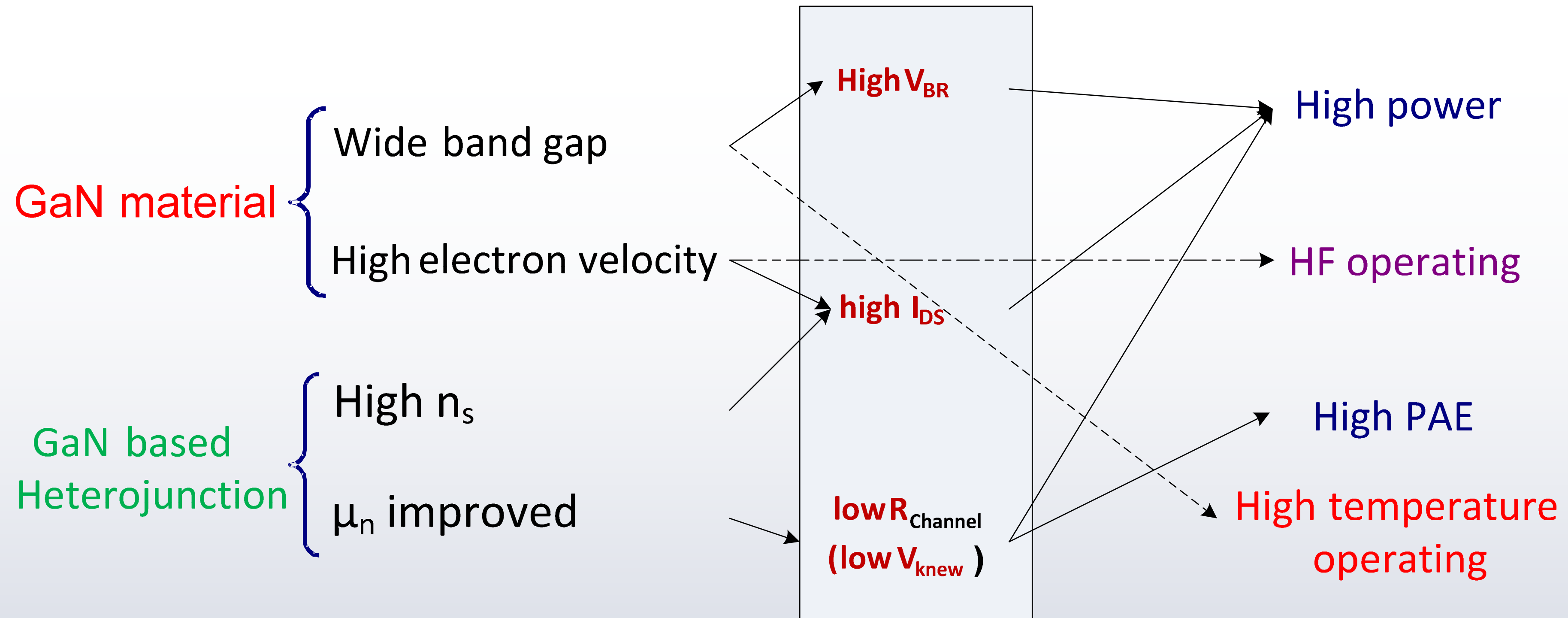
Material	T_{max} (°C)	λ (W/K.cm)
Si	300	1.5
GaAs	300	0.5
4H-SiC	600	4.5
GaN	700	1.3
Diamond	1000	20

→ 3 (bulk)

Why gallium nitride for power electronics?



Why a GaN-based heterostructure ?

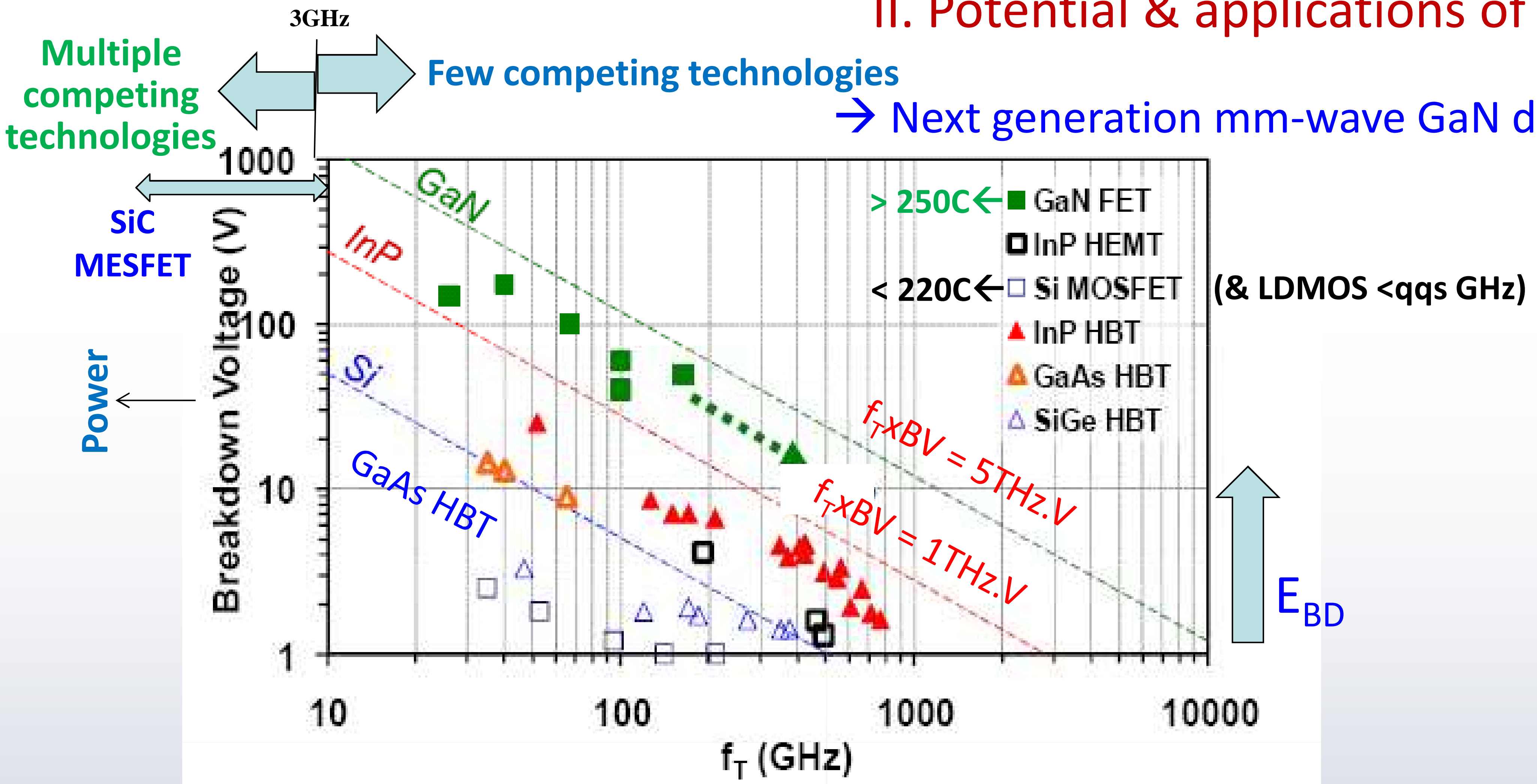


→ density, small size, easy impedance match

→ High output power simplified voltage conversion

→ Operation under extreme environmental condition

II. Potential & applications of GaN



- Higher operating voltages than traditional III-Vs and Si → robust and rugged mixed signal ICs

Advantages & Benefits
• **Linearity & Bandwidth -** Improved BW performance
• **Green -** More power efficient per mW of RF power
• **Power and Size -** More RF power per mm²
• **Opex/Capex -** Lower BOM and operating costs

- Higher efficiency
  - Reduce heatsink requirements, smaller size
  - Lower thermal, increase life expectancy
- Wide bandwidth
  - Replace 2 or 3 amplifiers with 1 amplifier
  - Improve engineering efficiency
- Improve reliability

Available substrate for the w-GaN growth

→ Need base lattice matched and good thermal conductivity

- ⇨ GaN and AlN free-standing from bulk material : < 2 inch, very expensive, doped, GaN S.I. in progress (<4 inch)
- ⇨ **SiC** : Expensive but nice lattice mismatch (<3%) …
- ⇨ Al_2O_3: Cheap but very poor thermal conductivity (test substrate or freestanding GaN from Al_2O_3 substrate)
- ⇨ Composites or hybrids substrates (carry over):
  - SopSiC, SiCopSiC: Oxide layer thermal barrier
  - Diamond single crystal or polycrystalline (deposit backside, -frontside)
- ⇨ Insulation metal oxides (tests), glass
- ⇨…
- ⇨ **Silicon**… (lattice mismatch of 17%)

Designing efficient quantum well heterostructures
Minimum strain / dislocations in the active region
→ The « hetero » substrate limits ?

Material	Thermal expansion coef. ($10^{-6}K^{-1}$)	K (W/K.cm)	Lattice constants (A)	Δa/a (%)
Si	2.6	1.5	5.43	17
Al_2O_3	7.5	0.3	4.75	14
4H-SiC	4.5	4.5	3.08	3
GaN	**5.6**	**1.3**	**3.19**	**0**
Diamond	0.8	20		

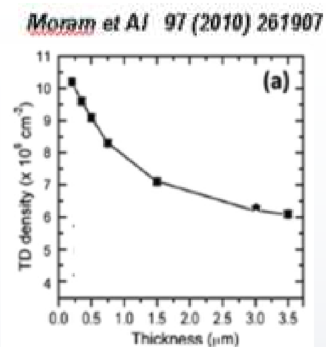
If all misfit dislocations emerge

→ max threading dislocation density = $1/a^2 \times (\Delta a/a)^2$

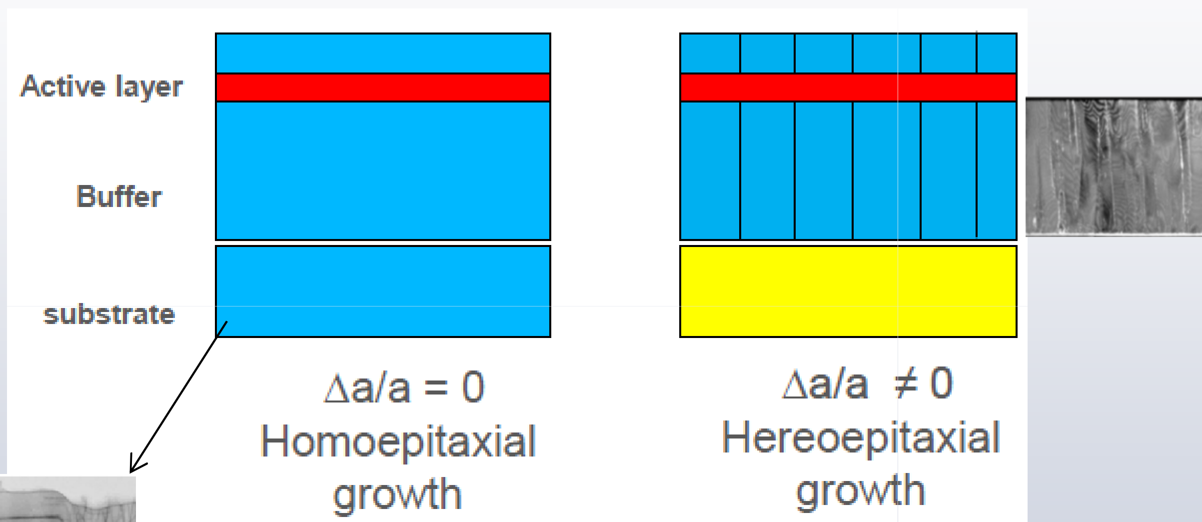
With $\Delta a/a = 10^{-3}$ → C° max = 10^9 /cm²...

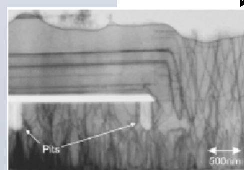
With $\Delta a/a = 10^{-2}$ → C° max = 10^{11} /cm²...

With $\Delta a/a = 10^{-1}$ → C° max = 10^{13} /cm²...

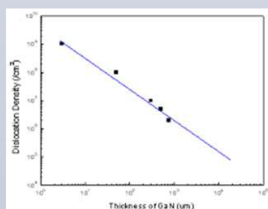


Progressive but very slow dislocation annihilation



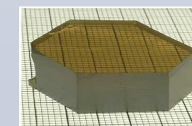


ELOG + HVPE
→ GaN freestanding



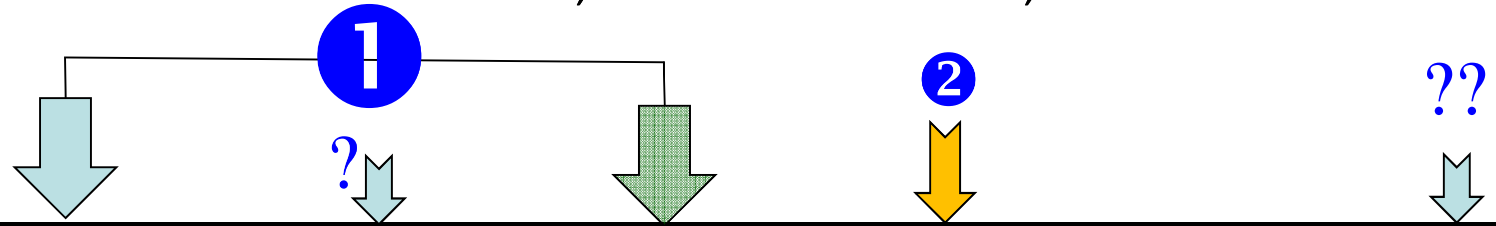
1µm GaN ←→10^6cm^{-2}

Or growth from solution HT (Ammono technique)... 1µm GaN ←→10^2cm^{-2}



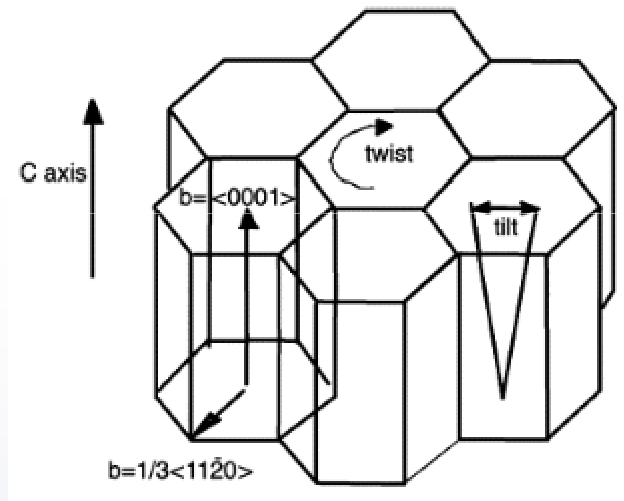
GaN template vendors or products

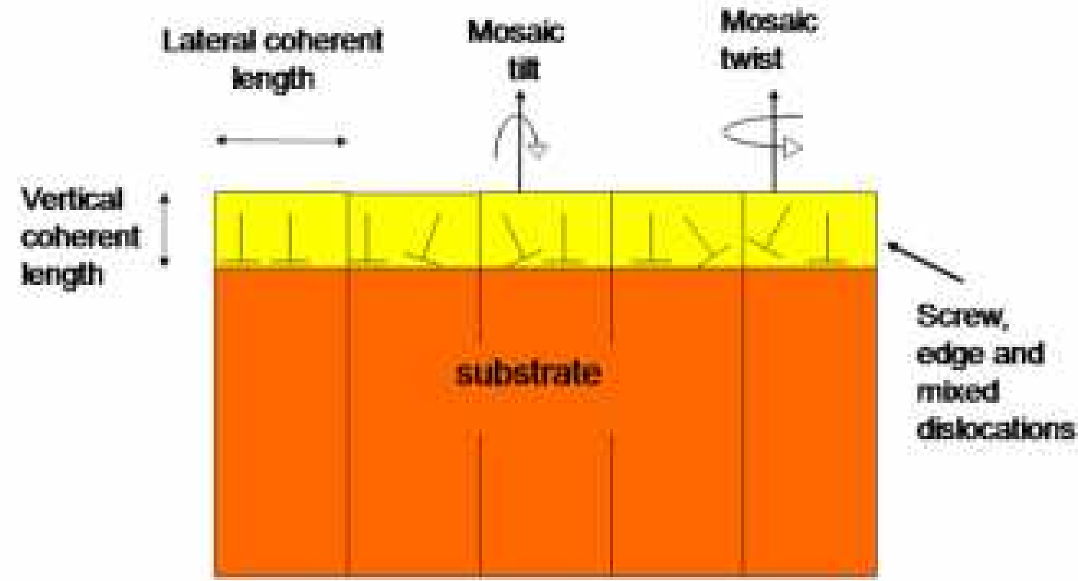
Substrates for GaN epitaxy and evaluation criteria: area, electrical insulation, cost…



	GaN / Sapphire	GaN / S.I. SiC	GaN / Bulk-GaN	GaN / Silicon	GaN / 3C SiC / Silicon	GaN / Glass	GaN / Diamond
Epiwafer providers	TDI Hitachi Cable NTT Kyma OptoGaN AZZURRO	CREE Hitachi Cable NTT Toyoda Gosei AZZURRO IQE,Kopin Picogiga	Sumitomo SEI Kyma LumiLOG Samsung-corning Hitachi Cable AZZURRO 1.5 pouce UHR SI GaN substrate 1G-1TΩ.cm, $10^4 cm^{-2}$	Nitronex AZZURRO Picogiga IMEC IQE NTT DOWA	Toshiba Ceramic (TOCERA)	BlueGlass	
Device maker	Lumileds Osram Nichia Toyoda Gosei Velox	CREE Fujistu RFMD NXP Freescale NEC, TriQuint	Sony Nichia NEC Toyota	**Nitronex** **OKI** **TriQUINT** **MicroGaN, ST,** **IR, Sanken,Fuji** **GaN system**	R&D	R&D	R&D
Application	Blue/white LED, power devices	RF devices	Blue/violet laser diode, power devices	Power devices ,RF,LED	RF devices Power devices	Blue/white LED	

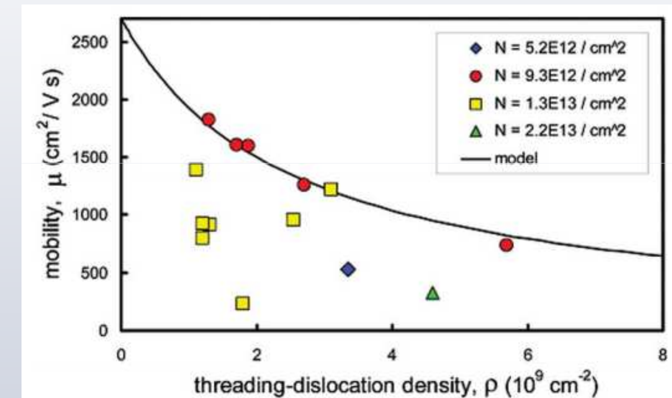
The « other » problem with heteroepitaxial growth of wurtzite materials
Tilt and twist → threading dislocations
Dislocations density : independant upon misfit but rather of nucleation





Screw threading disloc
→ Tilt accomodation

Edge threading dislocation
→ Twist accomodation

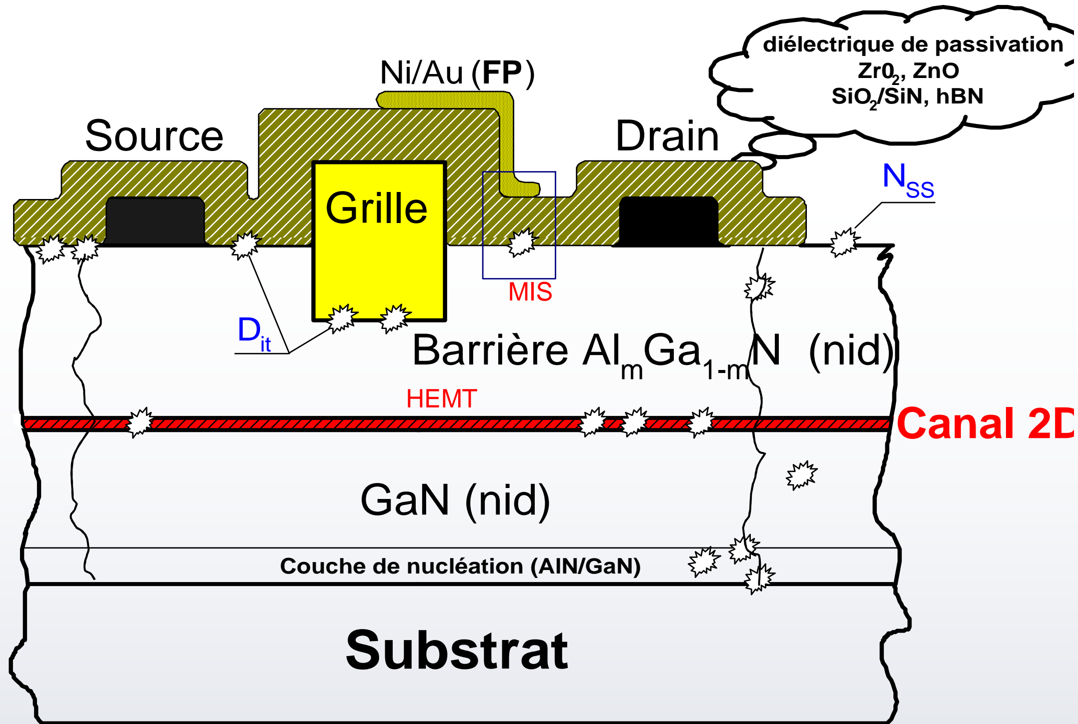


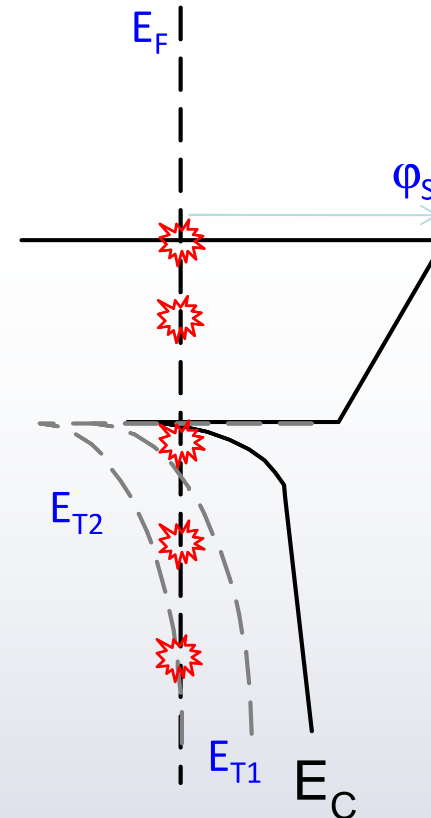
- **Lower misfit substrate are not enough to reduce dislocations density**

- **For cost reasons and material maturity → 2 solutions are possible : GaN on SiC and Si substrate**

N.V. Safriuk, *Semiconductor Physics, Quantum Electronics & Optoelectronics, 2013. V. 16, N 3. P. 265-272.*

Traps localisation



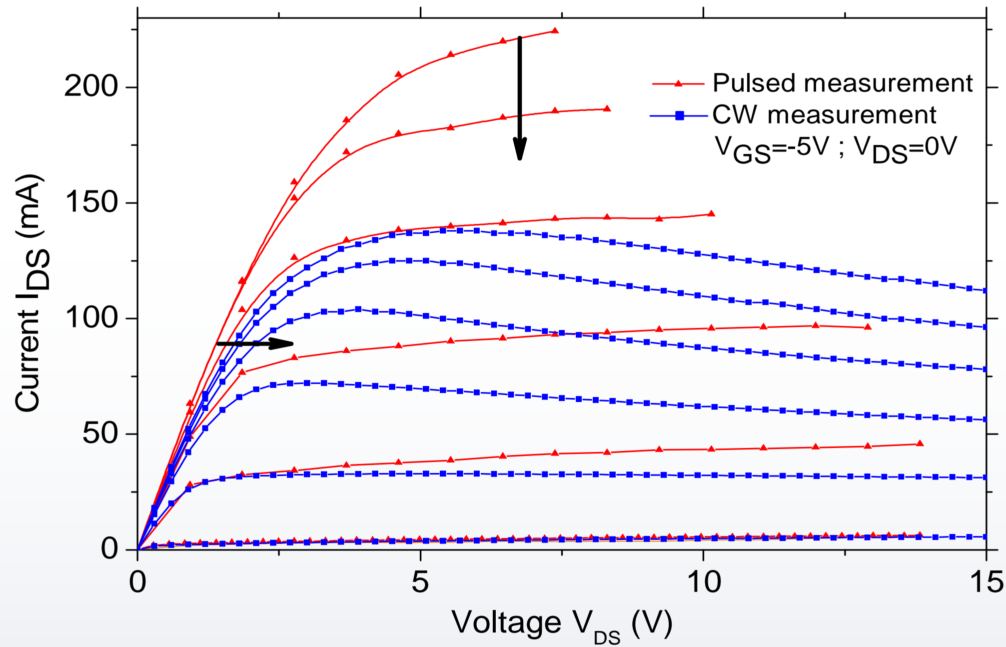


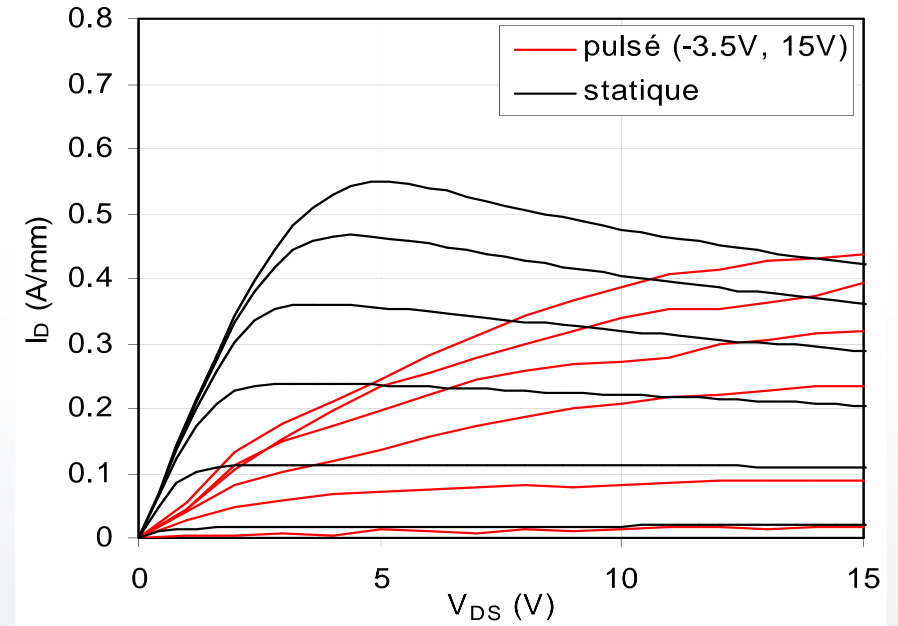
Traps located :

1. AlGaN free surface
2. Under gate
3. Passivated surface
4. Impureties in AlGaN bulk
5. Buffer GaN defects
6. Dislocations
7. Nucleation layers
8. Interfaces
9. SI Substrat

→ N_D^+ from the surface { V_N, O_N …from:
- ambient, moisture
- epitaxy (precursors and gases used)

Surface state dispersion





Degradation of transport properties due to self-heating

traps - surface states

+

Strain provided externally

Thermal management

Material engeenering + technological process

⇨ Why GaN on Si - Low cost
- Thermal conductivity similar to GaN
- High electrical resistivity
- Large area and highly qualified wafer availability (up to 8“ on GaN…)
- Different crystallographic orientations (111), (001), (110)
- MOS compatible (sophisticated silicon technology available micro-machining, fine lithography
- Facilitates transfer to exotic substrate (diamond, flexible, …)
- …

Difficulties:

1) Large lattice mismatch and different lattice structure
Poor hetero-interface, High density defects

2) Large difference of thermal expansion coefficients, cracking, bowing

3) Strong reaction between GaN and Si (Ga and Si meltback etching reaction)

How to resolve:

- Insertion of AlN and/or multilayered buffer layer
- Selective area epitaxy …

IV. Technological process

- Alignment marks (Ni/Mo) (others, cleaning and pre-passivation)

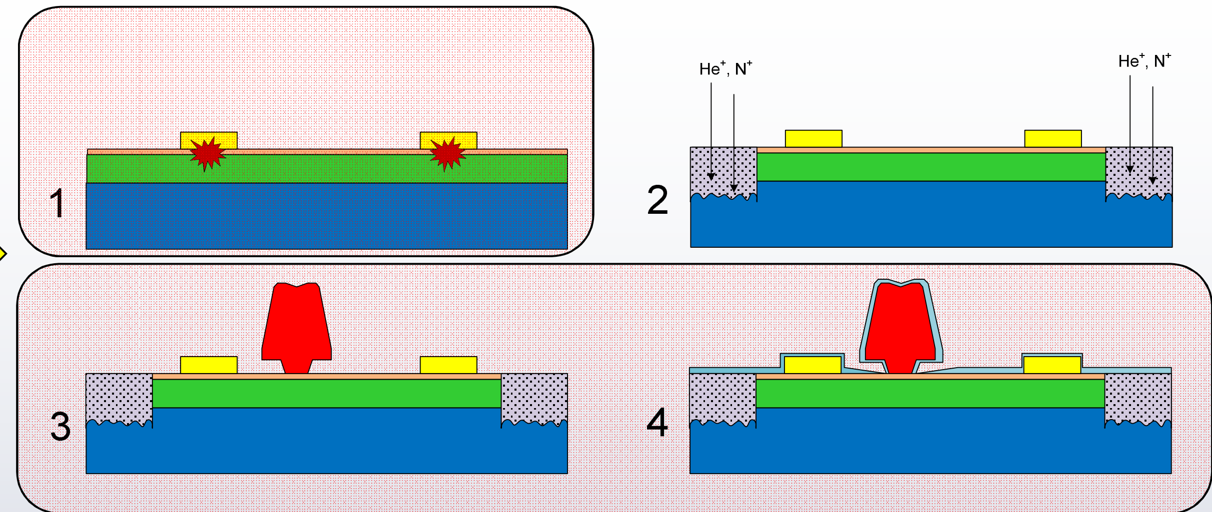
1. Source-drain ohmic contacts (with or Au-free…)
   and annealing (HT or LT, recess and n^{++}GaN re-growth)
2. Insulation components by implantation (He^+ or N^+)
3. T-gate or nitride-gate (Three or two resist layers process + recess or not)

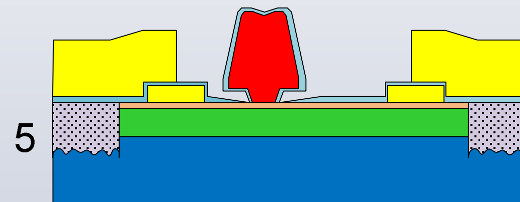
4 or 2’. Surface pretreatment and passivation (SiO_2, SiN, SiO_2/Si_3N_4…)

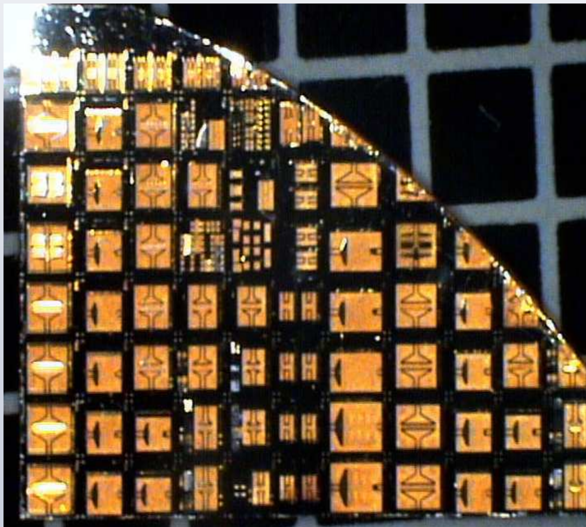
4’. Field plate (optional)

5. Thickening pads (Ti/Au or Au free)
6. BCB Level and air Bridge

Critical steps

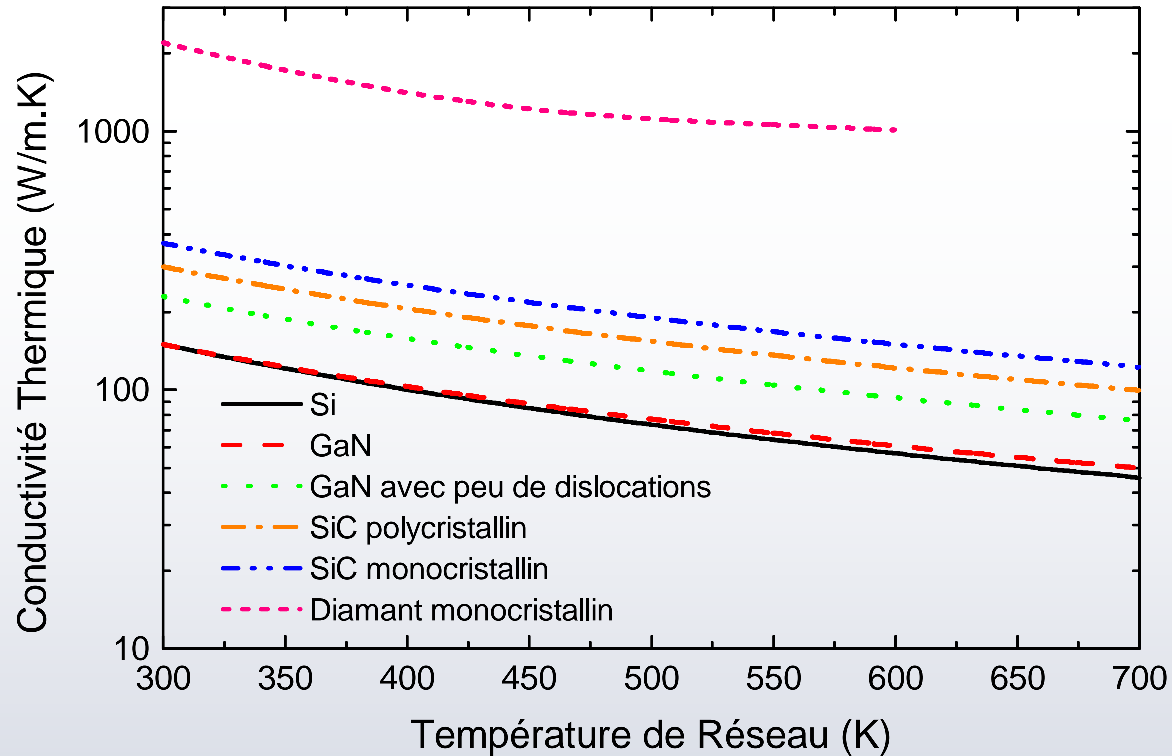






Silicon substrate
Buffer layer
Active area
Passivation layer
Ohmic contact
Schottky contact
Pads

Thermal conductivity

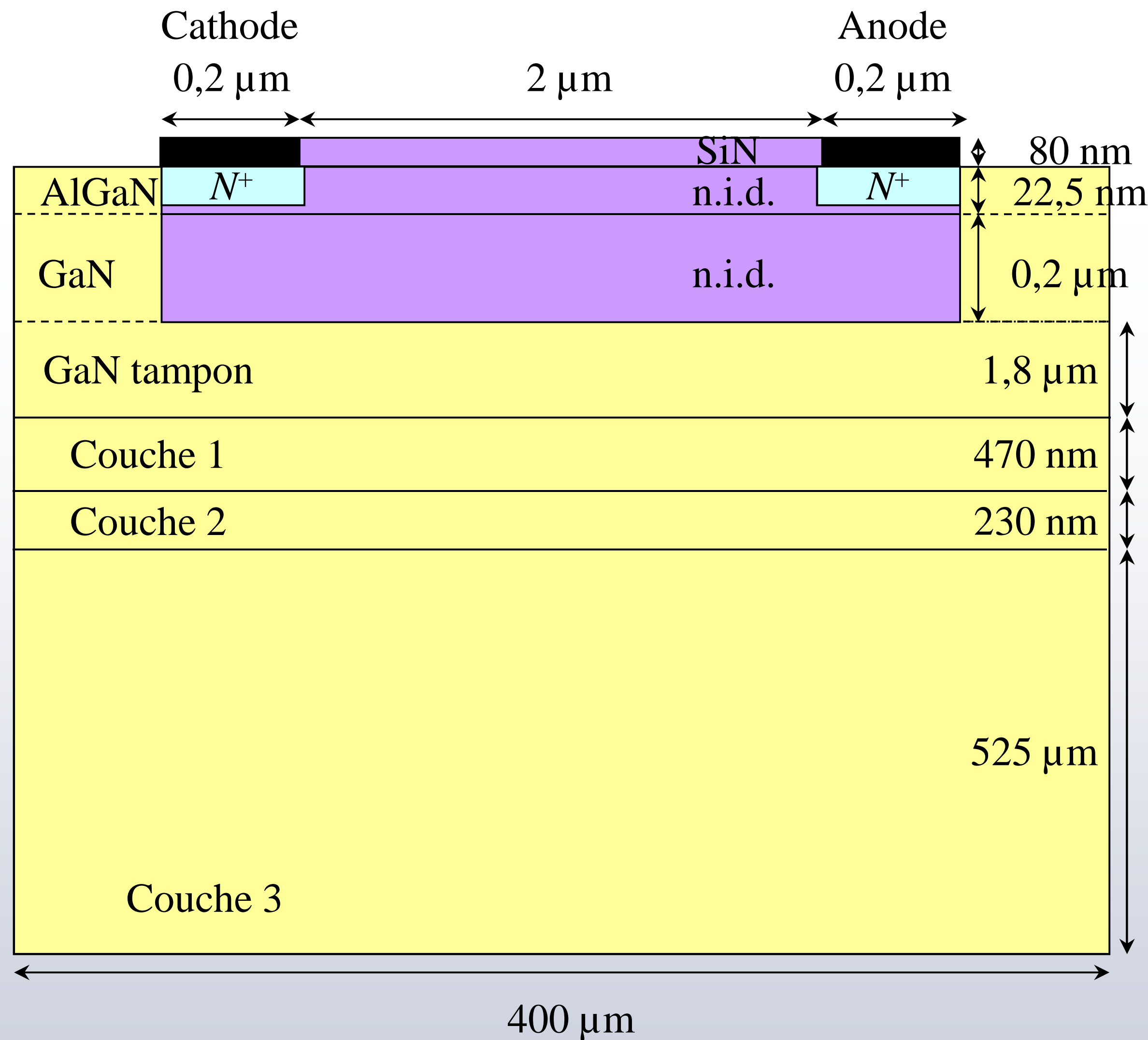


Conductivités thermiques pour chaque matériau à 300 K.

Matériau	κ_L (W/m·K)
Silicium	150
GaN avec 10^9 cm^{-2} disloc.	150
GaN avec peu de dislocations	230
SiC polycristallin	300
SiC monocristallin	370
SiO_2	1,4
Diamant polycristallin	2200
Diamant monocristallin	2400

→ Thermal conductivity decreases when the lattice temperature increases.

Thermal analysis of composites substrates



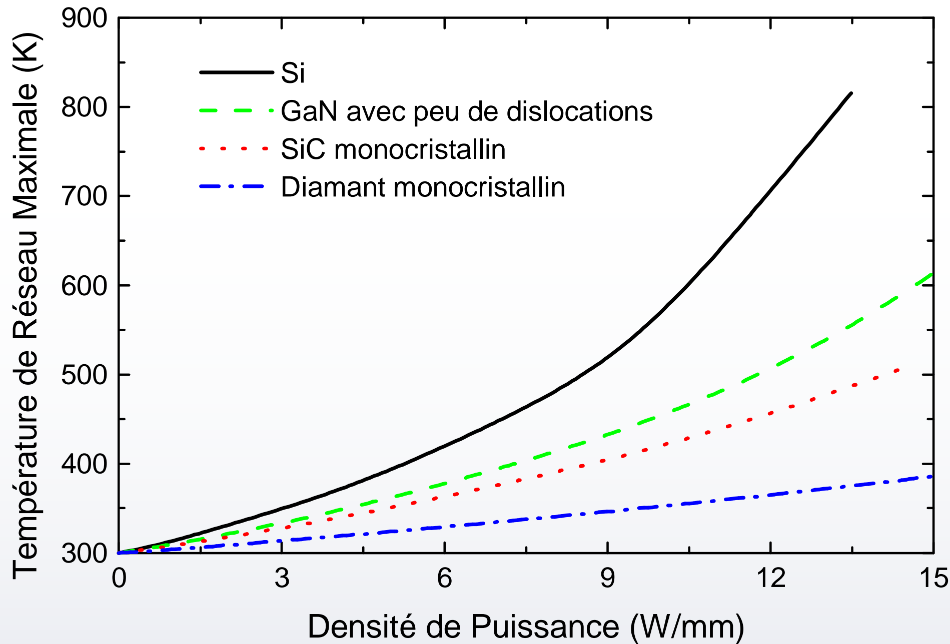
TLM $Al_{0.25}Ga_{0.75}N/GaN$

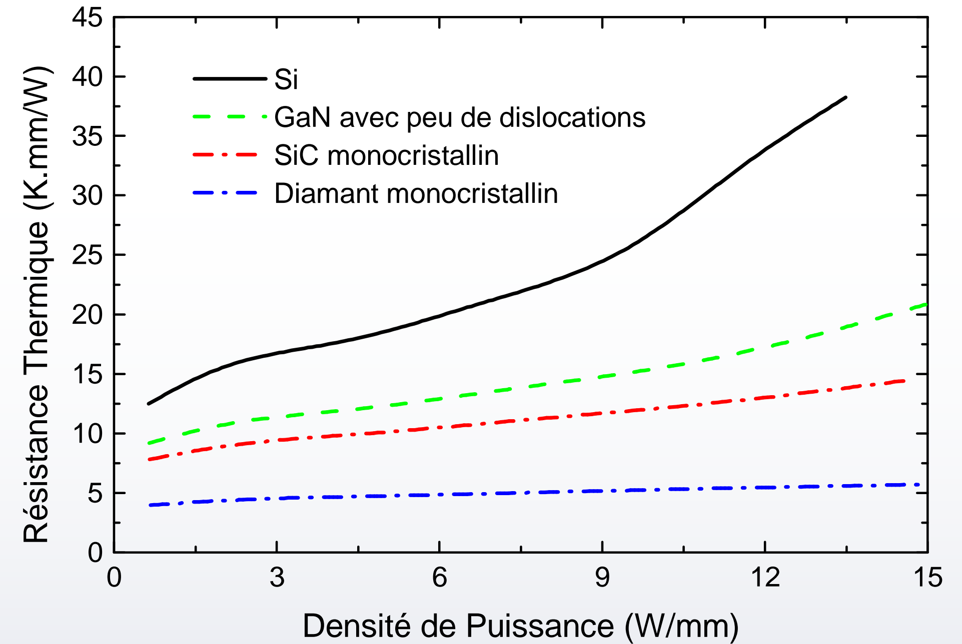
Substrats composites

Substrat	Couche 1	Couche 2	Couche 3
SopSiC	Si	SiO_2	poly-SiC
SiCopSiC	mono-SiC	SiO_2	poly-SiC
GaNopSiC	GaN	SiO_2	poly-SiC
Sopdiamant	Si	SiO_2	poly-diamant

Thermal performance

TLM AlGaN/GaN on bulk substrate

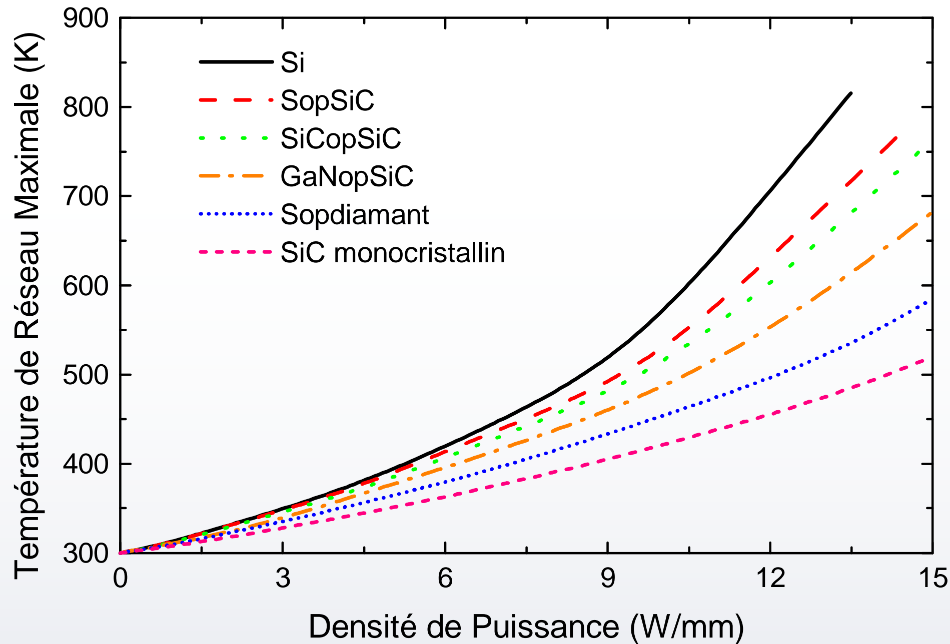


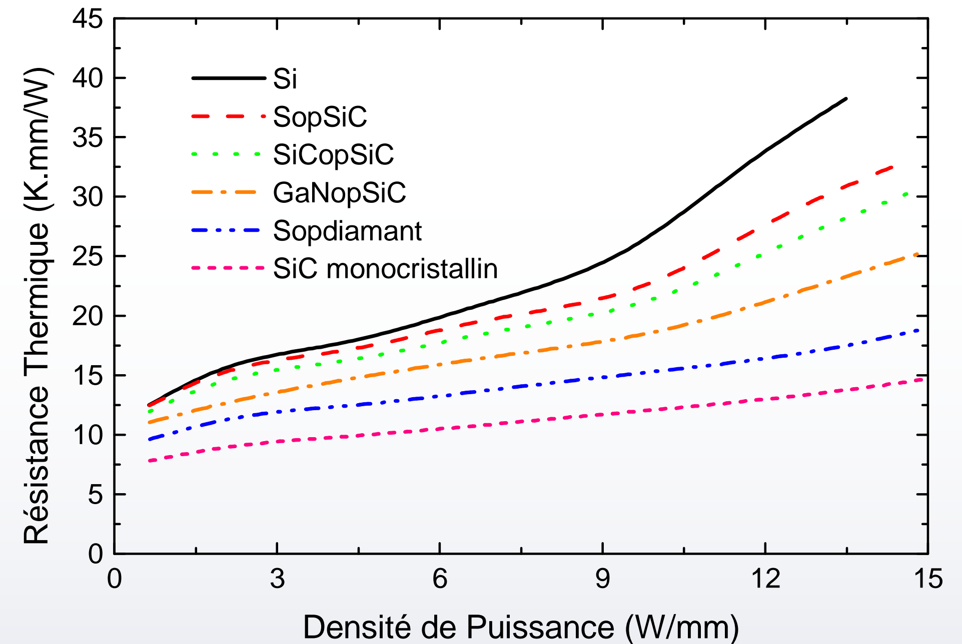


Substrat	Densité de puissance dissipée (W/mm)	R_{th1}(K·mm/W) simulation	R_{th2}(K·mm/W) simulation	R_{th}(K·mm/W) mesure
Si	7,5	21,8	20,8	21,2
GaN avec peu de dislocations	7,5	13,9	13,2	
SiC monocristallin	7,5	11	10	9,4
Diamant monocristallin	7,5	5	4,1	

Thermal performance

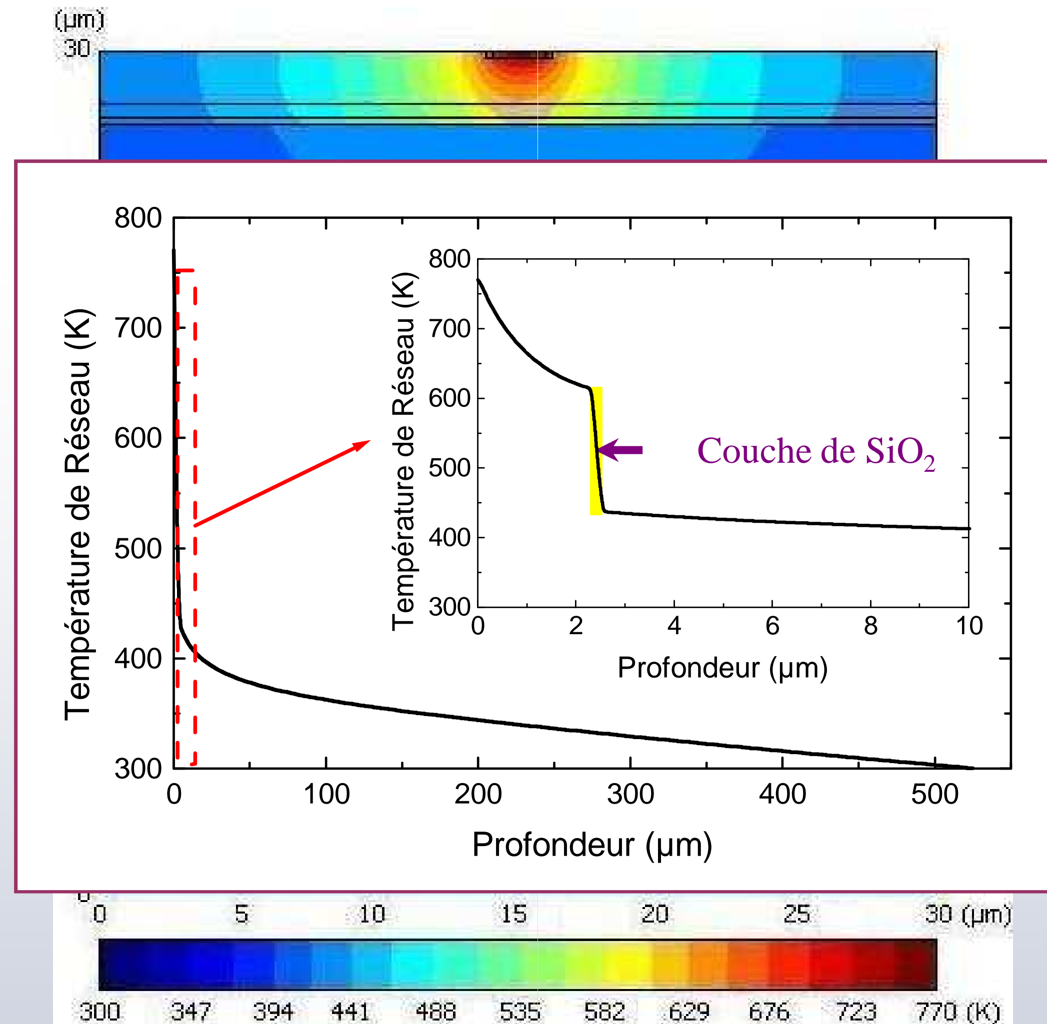
TLM AlGaN/GaN on bulk substrate





Substrat	Densité de puissance dissipée (W/mm)	R_{th1}(Kmm/W) simulation	R_{th2}(Kmm/W) simulation	R_{th}(Kmm/W) mesure
SopSiC	7,5	20,2	18,9	18,1
SiCopSiC	5	16,7	15,8	15,9
GaNopSiC	7,5	16,8		
Sopdiamant	7,5	14		

Example: Lattice temperature profil for SiCopSiC substrate



- With InAlN or AlN barrier, → n_s is greater

→ Need for a heat conductive substrate is more important

- The choice of the bonding technique defines success of the heat dissipation

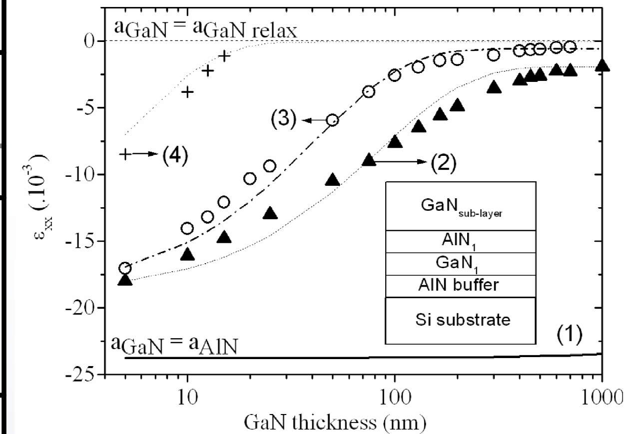
VI. Comparison of AlGaN/GaN heterostructure on Si substrate

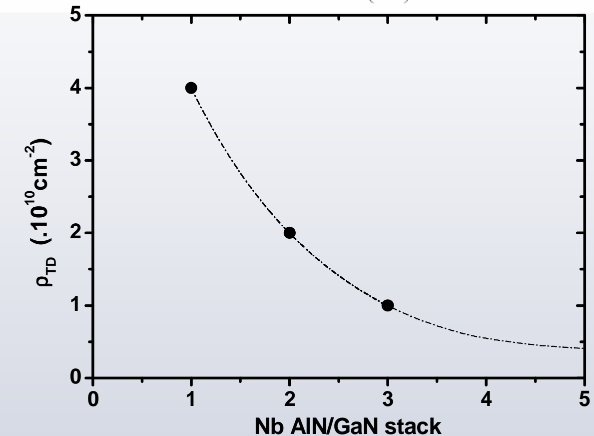
AlN exclusion layer :
↘ alloy scattering
↗ electron mobility

Mitigating stress layers

Layer	Thickness
GaN	3 nm
$Al_{0.29}Ga_{0.71}N$	21 nm
AlN	1 nm
GaN	1.73 µm
AlN	250 nm
$Al_{0.15}Ga_{0.85}N$	250 nm
AlN	43 nm
Si (110) substrate Si (111)	

Layer	Thickness
GaN	1 nm
$Al_{0.24}Ga_{0.76}N$	25 nm
AlN	1 nm
GaN	0.8 µm
$(AlN/GaN)_3$	1.2 µm
Si (001) substrate Si (111)	



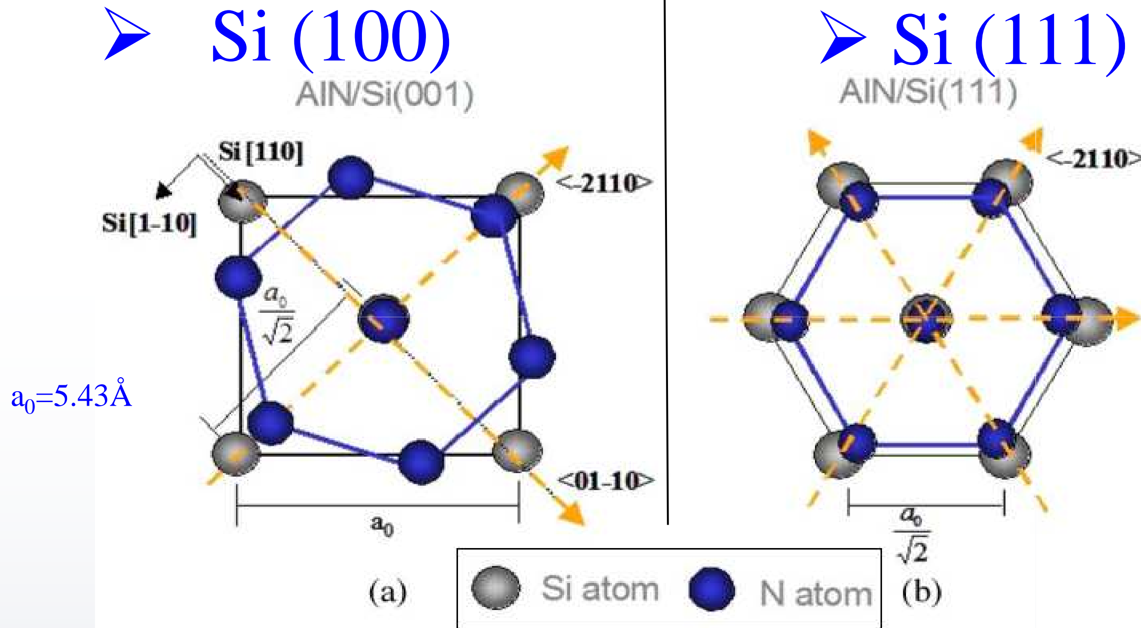


Cross section view of HEMT structures grown on silicon substrate

GaN growth on Si substrate oriented(100), (111) and (110)

→ Top view of w-AlN lattice, Si(001) and Si(111) in the growth direction [1]

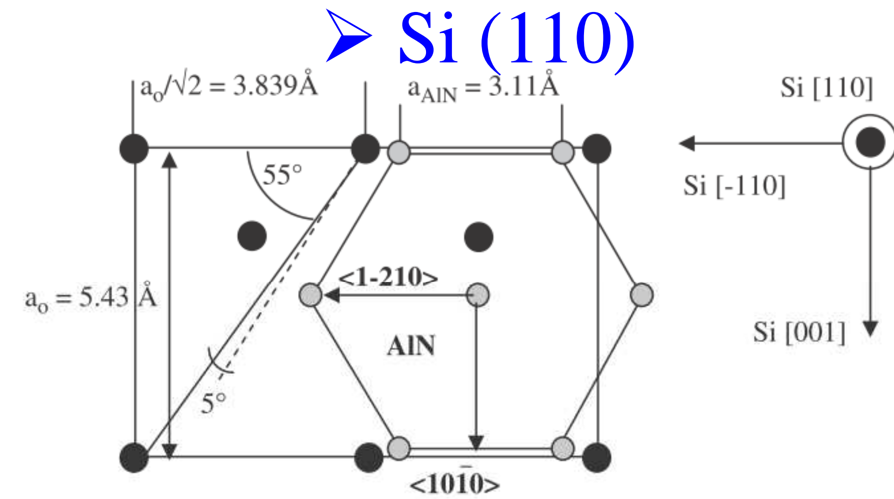
➢ Si (100) ➢ Si (111)

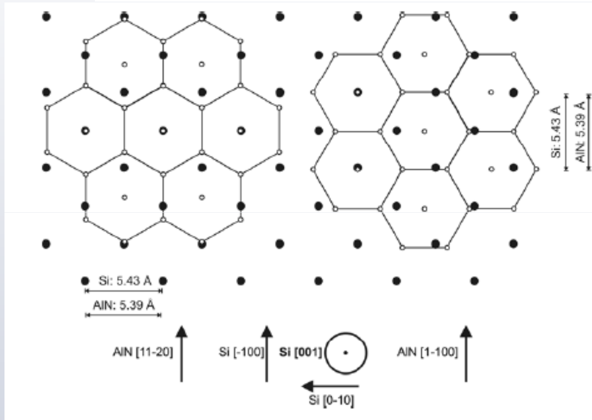


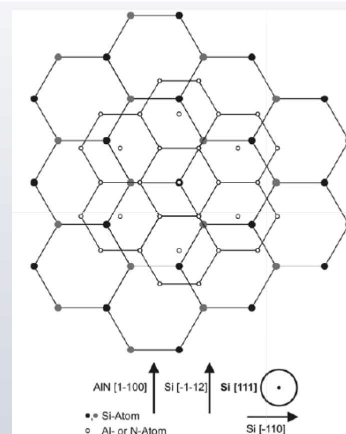
a_0=5.43Å

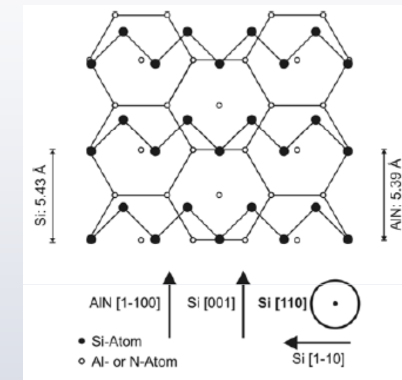
→ Top view of w-AlN lattice and Si (110) surface in the growth direction [2]

➢ Si (110)









Square symetry surface + 2 aligned domains alternatively rotated by 90°
→ Necessitate misorientated substrates of a few degrees

Hexagonal threefold symetry surface
→ Suitable with w-GaN

Si surface is not isotropic
→Offers a unique in-plane orientation quasi lattice-matched with AlN in one of the in-plane directions

[1] J.C. Gerbedoen *et al. IEEE Trans. Elect. Dev.* **57** 7 (2010)1497-1503.
[2] Y. Cordier *et al.*, Phys. Stat. Sol. C **6** S2 (2009) S1020-S1023.

VI. Comparison of AlGaN/GaN heterostructure on Si substrate

Structural properties comparison of GaN/Si

GaN on	GaN Thickness (μm)	Roughness rms (nm)	ε_{xx}	Dislocations density ($\times 10^9$ cm^{-2})	Residual doping ($\times 10^{13}$ cm^{-3})	FWHM XRD (002) (arcsec)	FWHM XRD (302) (arcsec)	Substrate bow (μm)
Si(001)	0.8	7-8	7×10^{-3}	11	400	1440	3100	-100
Si(110)	1.7	5	**5×10^{-4}**	**3**	**10**	900	**1600**	**47**
Si(111)	1.7	5	**$1\text{-}6\times10^{-4}$**	3.2-7	7-200	**700**	1900	**-10 to +40**

Properties of w-GaN layers grown on 2-inch silicon substrates with (001), (111) and (110) orientations [1]

[1] Y. Cordier *et al.*, Phys Stat. Sol. C 6 S2 (2009) S1020-S1023.

Si (001) → Orientation mainly used in silicon technology
→ Growth of w-GaN is more difficult
→ Limit the GaN buffer thickness to 1μm due to large thermal expansion coefficient.

Si (111) → More suitable for the epitaxial growth of the wurtzite phase

Si (110) → Compatible with MOSFET realization
→ Surface roughness & surface morphology very similar to the ones obtained on Si (111)

☺ (110)-oriented silicon substrate presents a strain state and a quality equivalent to the one obtained on Si(111) and high quality AlGaN/GaN heterostructures can be grown

VI. Comparison of AlGaN/GaN heterostructure on Si substrate

Transport properties comparison of GaN/Si (→ 2013)

HEMT	R (Ω/)	μ_n (cm²/V.s)	n_s ($\times 10^{12}$cm⁻²)
Si(100)	440/352*	1800/1718*	8/10.4*
Si(110)	340/**245***	2150/**2045***	8.5/**12.1***
Si(111)	355/300*	2160/2000*	9/10.6*

Low-field transport properties for HEMTs on Si(100) and Si(110) substrates.
Stars indicate results obtained on the same devices after passivation.

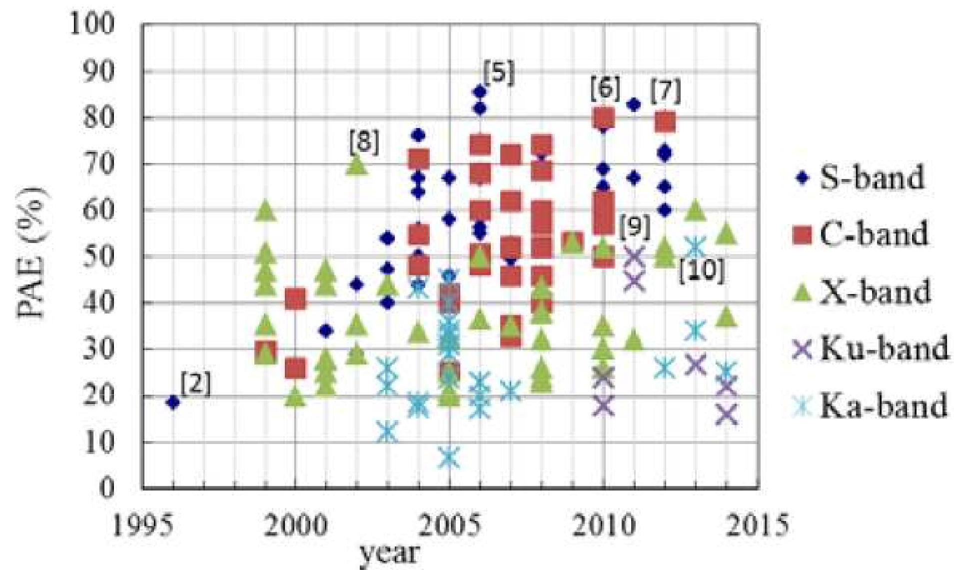
VI. Comparison of AlGaN/GaN heterostructure on Si substrate

Best power results on different Si substrates

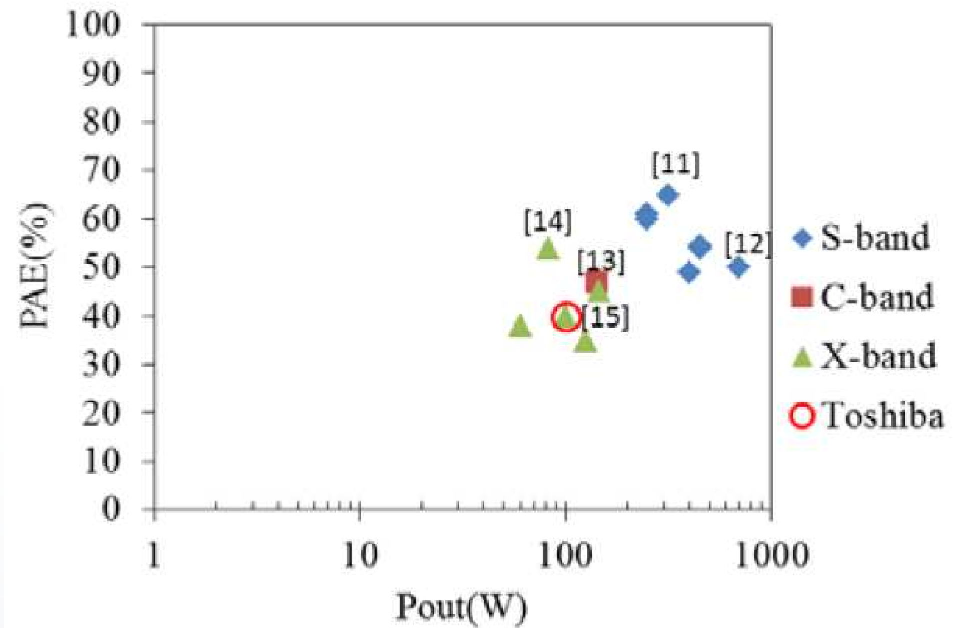
HEMT	frequency	Gp (dB)	P_{1dB} (dBm)	Psat (dBm)	Psat (W/mm)	PAE (%)	V_{GS0}, V_{DS0} (V)	W (μm)	Measurement condition
On Si(100)	@ 4GHz	19.3	20.75	25.3	**3.4**	14.3	(-2,+25)	2×150	Pout $_{max}$
		22.8	18.3	25	3.15	**22.9**	(-2,+20)	2×150	PAE-P_{out}
	@10GHz	7.5	22.1	29.4	**2.9**	20.4	(-2,+30)	2×150	Pout $_{max}$
		14.9	23.2	29	2.65	**22.2**	(-2,+25)	2×150	PAE-P_{out}
On Si(110)	@18GHz	15.6	20.3	23.4	**3.76**	33	(-3,+15)	2×30	Pout $_{max}$
		20.3	14.2	21.6	2.4	**40**	(-3,+10)	2×30	PAE-P_{out}
	@ 40GHz	10.6	18.4	23	**3.3**	**20.1**	(-3.3,+15)	2×30	-
On Si(111)	@18GHz	9.1	24	27.1	**5.1**	20	(-4,+35)	2×50	-
	@ 40GHz	9	17.8	21	**2.7**	18	(-1.6,+15)	2×25	-

AlGaN/GaN
on Si(111)
on Si(100)
on Si(110)
InAlN/GaN on
Si (111)
AlN/GaN on
Si(111)
AlGaN/GaN/GaN
AlGaN/GaN/SiC
InAlN/GaN/SiC
AlGaN/GaNSiCopSiC
P_{out} (W/mm)
frequency F_T (GHz)

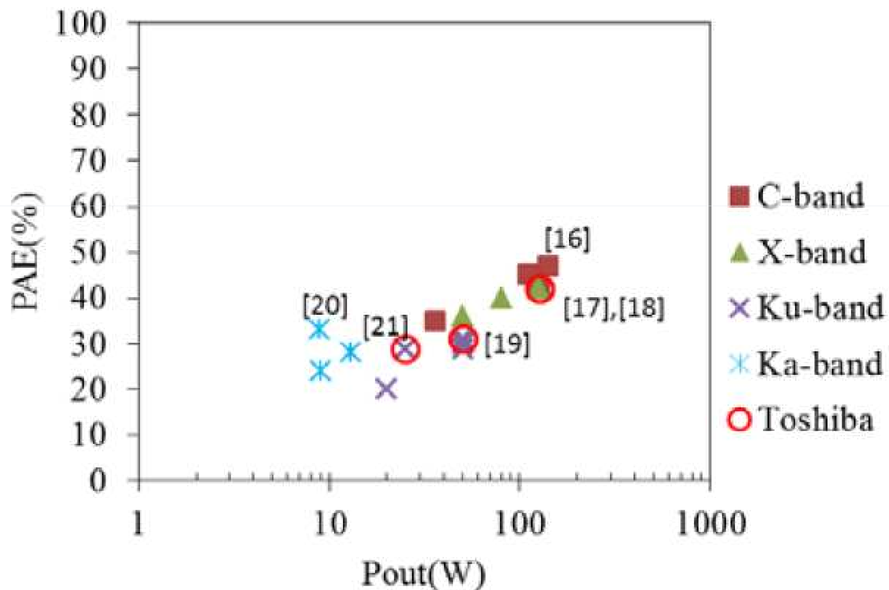
Comparison PAE between HEMT on SiC et Si



PAE of AlGaN/GaN HEMTs versus year.



PAE of recent AlGaN/GaN HEMTs products for radar systems versus Pout.



PAE of recent AlGaN/GaN HEMTs products for satellite communication systems versus Pout.

PAE GaN on SiC > PAE GaN on Si of 20 % min in Ka band

NF_{min} GaN on SiC like GaN on Si

Kazutaka Takagi Asia-Pacific Microwave Conference 2014

Expanding interest in cubic silicon carbide (3C-SiC) on silicon substrate

SiC → material very attractive but **too expensive**

Alternative pathway, dév. 1990 → SiC/Si from ∅ **150mm to 300mm**

Cree of Durham, NC, USA. MTI Corp of Richmond, CA,USA is one commercial supplier of 3C-SiC on Si wafers with diameter of up to 8-inch (200mm).

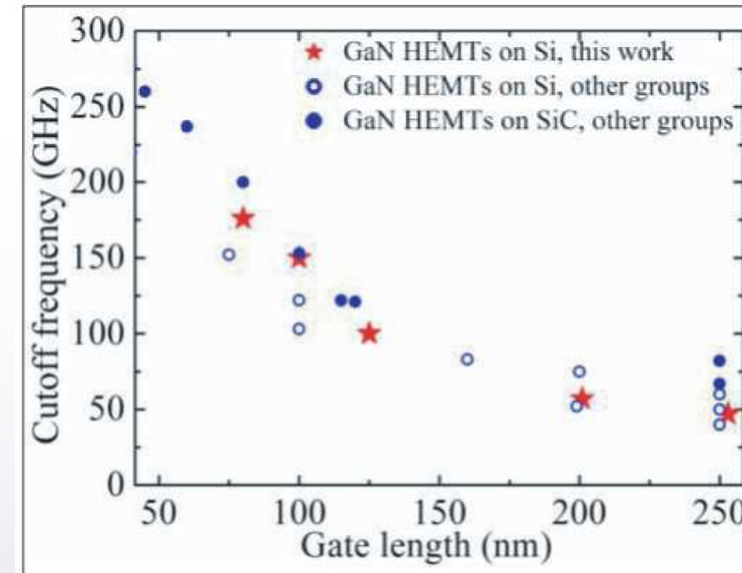
Cost analyses → process should add **no more than $35 to the cost of 300mm** substrates.

QMF claims 1% uniformity in SiC layer thickness across 300mm wafers.

Anvil Semiconductors Ltd of Coventry, UK claims 'unique technology' for growing 3C-SiC on silicon that reduces SiC wafer **costs by a factor of 20**

VII. β-SiC/Si : 3rd possible way

Air Water Inc., an Osaka-based supplier of gases for industrial and medical applications, has developed mass-production technology for **low-cost 8-inch SiC and 6-inch GaN wafers (GaN/3C-SiC/Si)** → **2014**



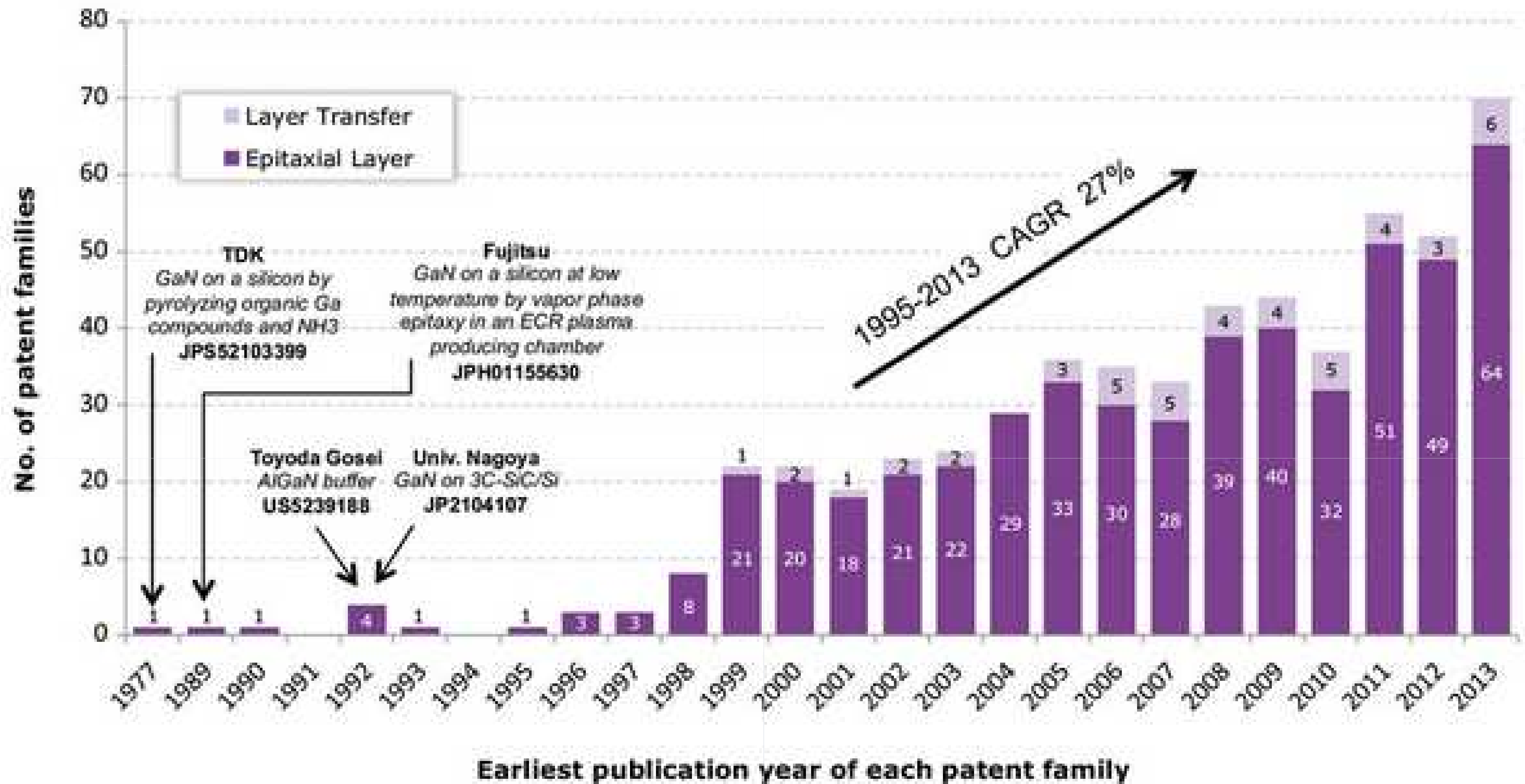
Comparison of cutoff frequencies of GaN HEMTs on Si with AlGaN barrier design A with best data reported by other groups for GaN HEMTs on Si and on SiC.

6インチ GaN on SiC/Si基板のXRC(X線ロッキングカーブ) 評価例

成膜構造	2 μm厚GaN(0001)/1.5 μm窒化物バッファ/SiC(111)/Si-sub.
Si下地基板厚	900 μm
Warp/Bow	≦90 μm
膜厚(GaN最表層)	2.0±0.5 μm
XRC FWHM	GaN(0004)≦700 arcsec GaN(10-12)≦1000 arcsec
クラック	≦5本 (EE5 mm)

For 6- to 8-inch wafer fabrication, the Azumino plant has a **monthly capacity of 2000 wafers**.
For 2-inch wafer fabrication, it has a capacity of 16,000 wafers a month.

http://www.awi.co.jp/business/new/sic/gan.html


Time evolution of patent publications
(Source : GaN-on-Silicon Substrate Patent Investigation, Yole Développement, April 2014)
Layer Transfer
Epitaxial Layer
No. of patent families
Earliest publication year of each patent family
TDK
GaN on a silicon by pyrolyzing organic Ga compounds and NH3
JPS52103399
Fujitsu
GaN on a silicon at low temperature by vapor phase epitaxy in an ECR plasma producing chamber
JPH01155630
Toyoda Gosei
AlGaN buffer
US5239188
Univ. Nagoya
GaN on 3C-SiC/Si
JP2104107
1995-2013 CAGR 27%
0
10
20
30
40
50
60
70
80
1977
1989
1990
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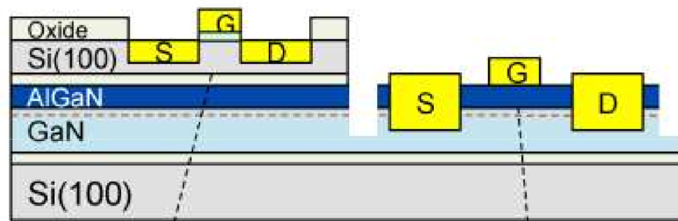
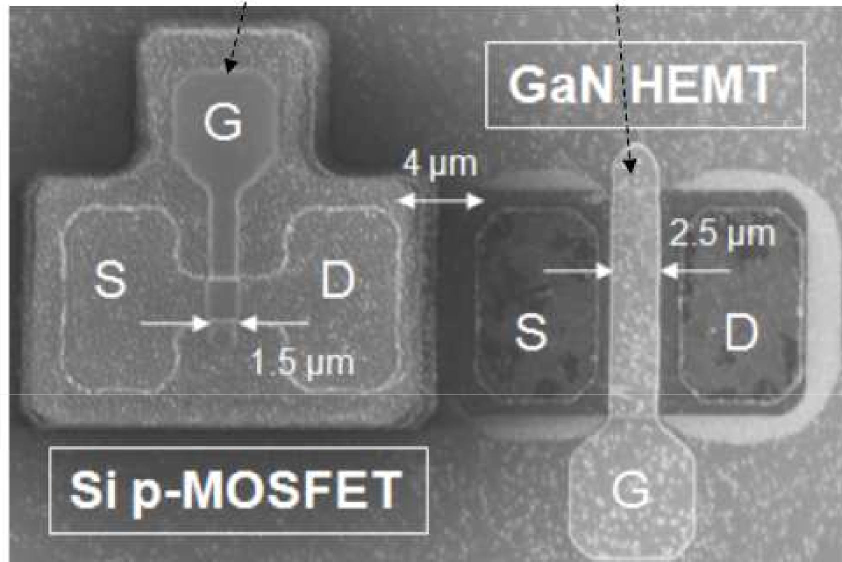
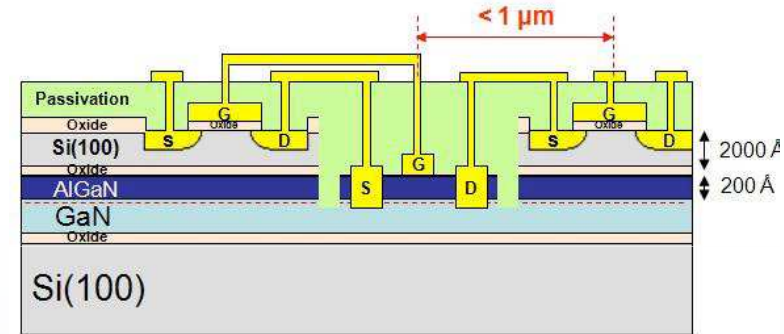
2013

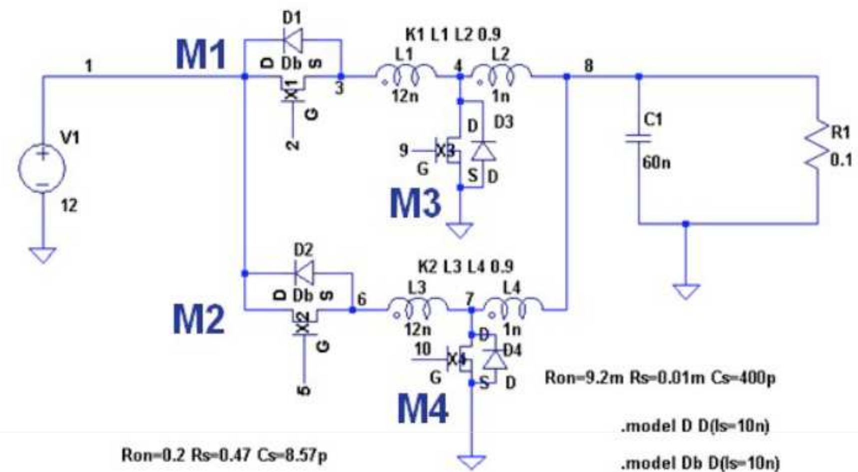
Hybrid Chips of Gallium Nitride and Silicon (100)

Digital gate realization







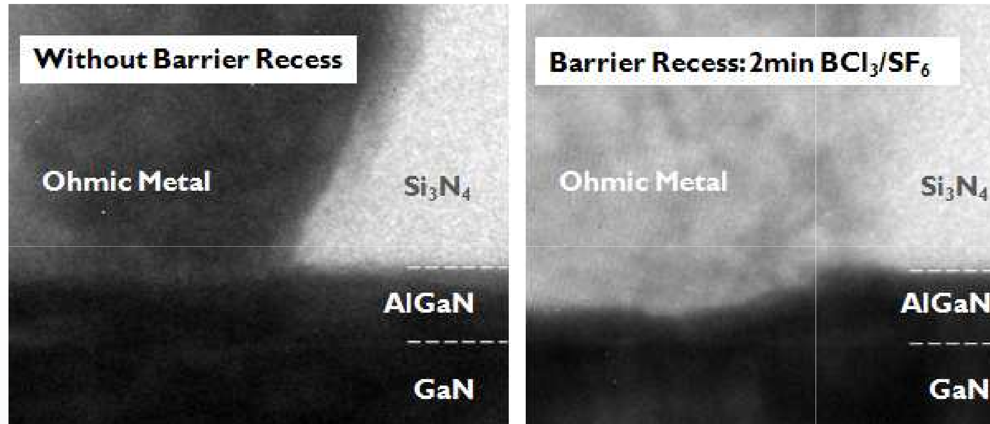


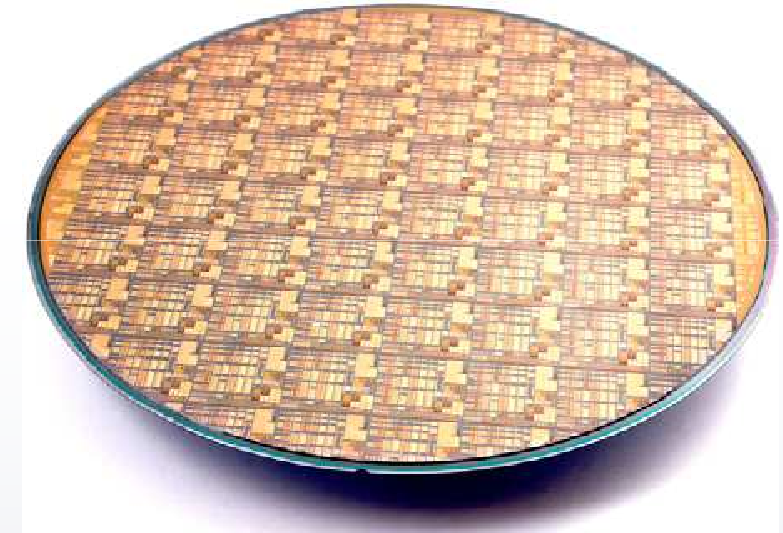
Circuit schematic of the new GaN-Si hybrid power converter. M1 and M2 are GaN-based power transistors while M3 and M4 are Si MOSFETs

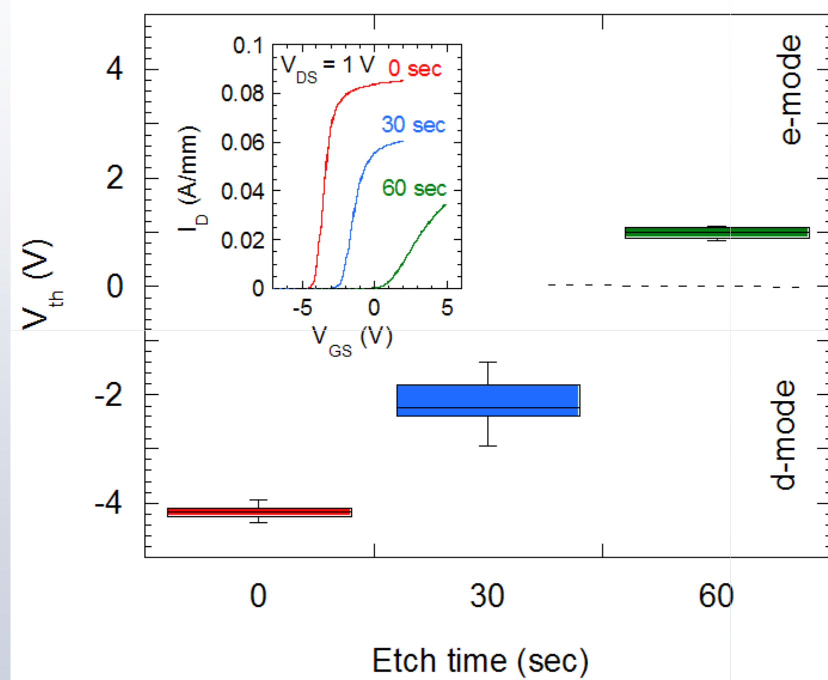
→ This process requires a transfer of layers

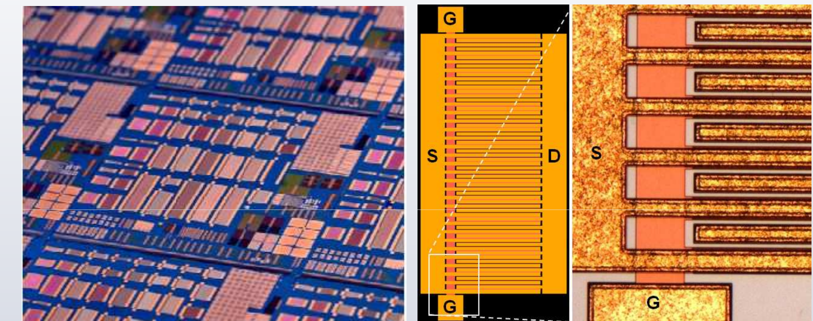
"Seamless On-Wafer Integration of Si(100) MOSFETs and GaN HEMTs," Jinwook W. Chung, Tomás Palacios, et al, IEEE Electron Device Letters, October 2009

Monolithic microwave integrated circuit GaN on Silicon (111)









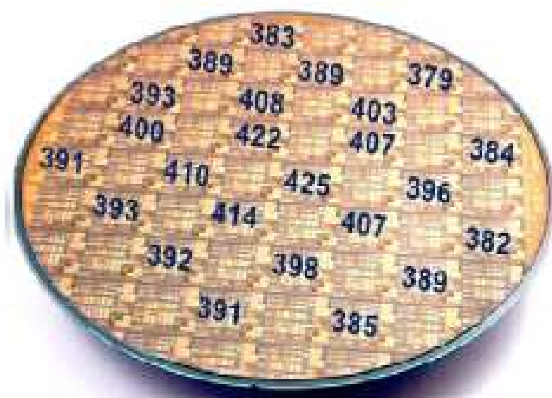
Photographs of a fully processed 200 mm GaN-on-Si MISHEMT device wafer

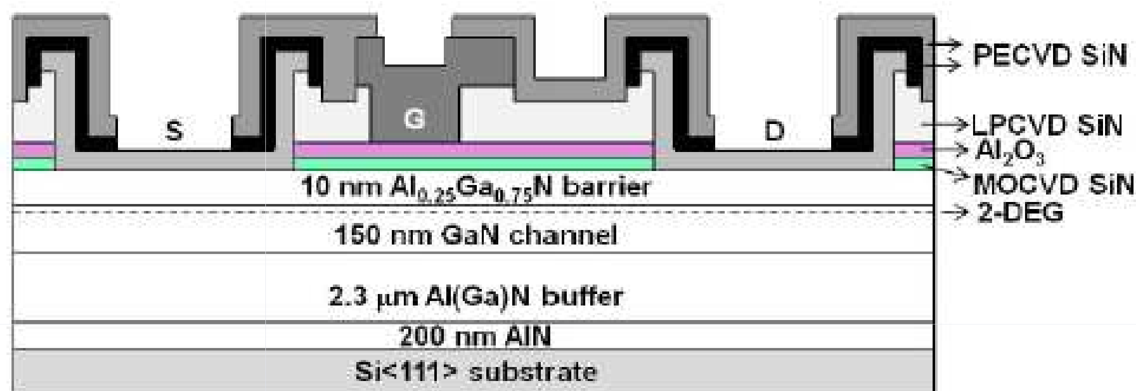
Au-free CMOS-compatible AlGaN/GaN HEMT processing on 200 mm Si substrates

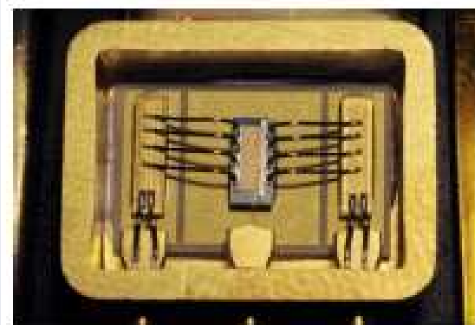
B. De Jaeger et al., Proceedings of the 2012 24th International Symposium on Power Semiconductor Devices and Ics (2012) - Bruges, Belgium

Development of wide band gap processing techniques compatible with a Si production environment "GaN in the line"

- ESA funded project to develop GaN on silicon power transistors using a Si CMOS compatible processing line
  - Fabrication on 150mm diameter silicon wafers for low cost
  - Novel Au free process, bi-layer insulated gate dielectric
  - Electrical performance and SEE radiation assessment



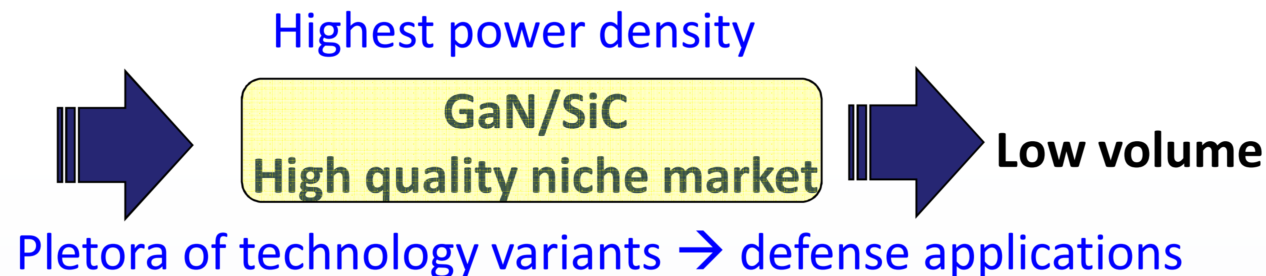




European Space Agency

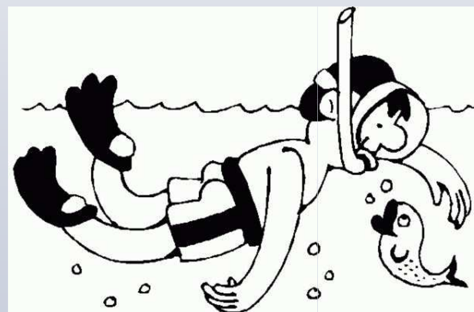
GaN HEMT on (Si vs SiC) ?

Bad:
PAE GaN on SiC > PAE GaN on Si
Linearity, reability better on SiC
....



BUT !...
Power density of GaN/Si is 8× better that GaAs with PAE to as much as 70% (*)
GaN/Si performance has matched that of GaN/SiC, which more expensive
NF_{min} (GaN/Si)<1.2dB to 40 GHz like GaN/SiC

SiC grows **200× to 300×** slower than **Silicon**



vs

GaN/SiC → perpetually **higher cost**

(*Internal MACOM calculations and projections of BO Cui, ECE, U. of Waterloo)

IX. Some remarks

→ Results of this inventory not limited
→ Today, GaN is poised to make the transition from an esoteric (government funded technology) to a high volume commercial mainstay

This transition need :
- technical merits clearly demonstrated on Si substrate
- tapping into large commercial markets that drive economies of scale
  (example: market of cellular handset)

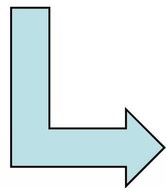
→ GaN/SiC has been produced by 3″ for cellular handsets, which today are attack from CMOS due to cost efficiencies

→GaN/SiC has no clear viable roadmap to large diameter

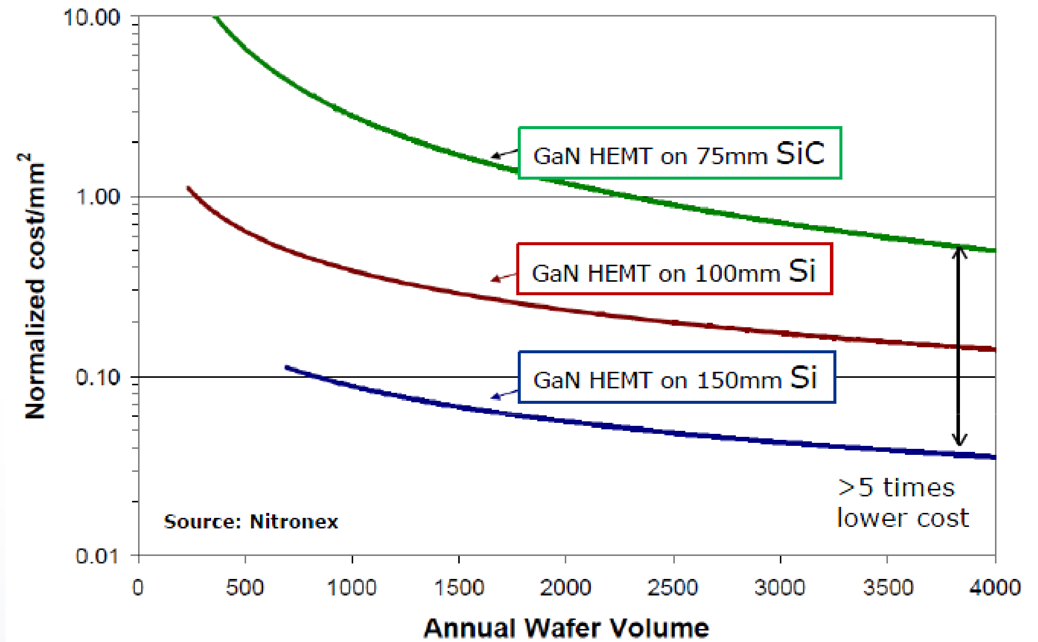
→ GaN/Si 8″ with RF demand and DC power market → 10× reduce in cost

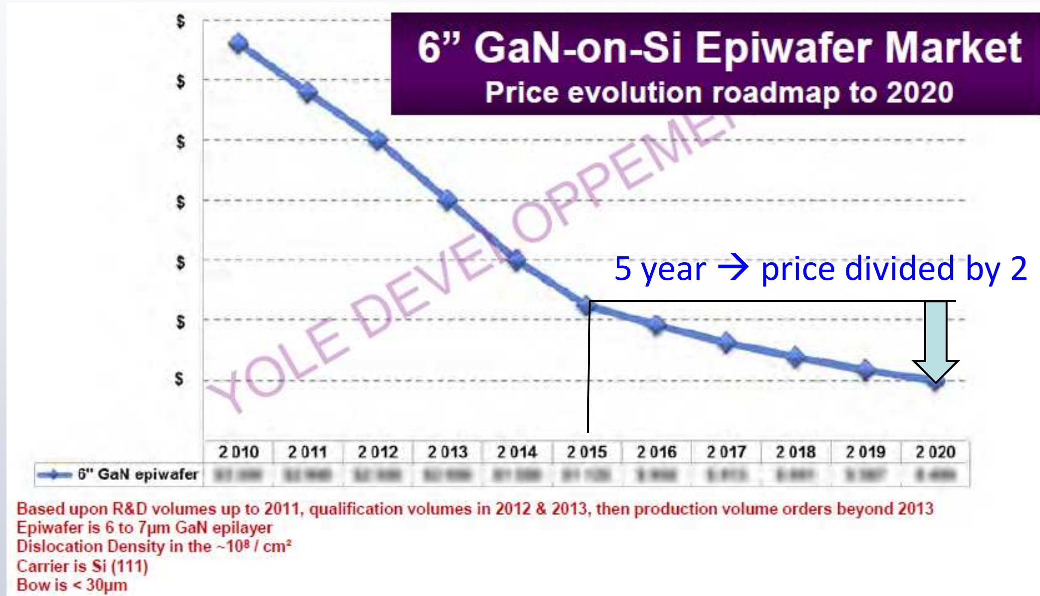
Why manufacture GaN on silicon ?

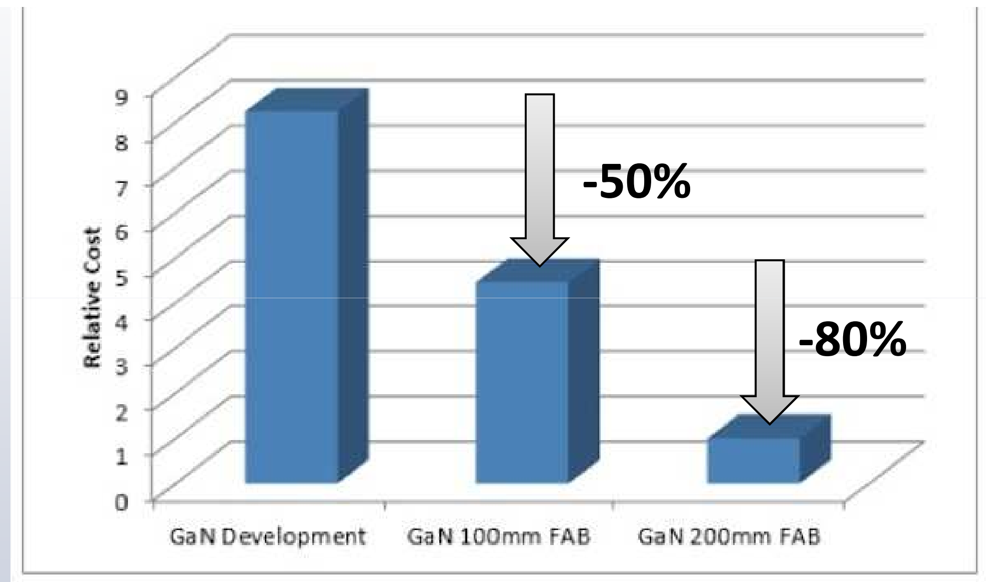
Cost sensitive applications → 8″



GaN/Si
mass production
Consumer applications







Hope → Intermediate solution : hybrid substrate 3C-SiC/(11X)Si ?

Thank you for your attention