>> Designing complex Frontend Modules for Ka-Band and WiGig communication using XPU-Technology

Contact:

W. Simon

E-Mail:simon@imst.com

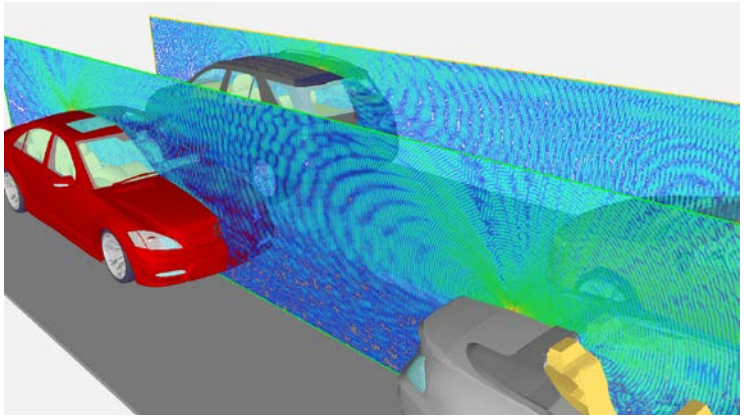
Outline

- Introduction
- XPU Technology
  - Overview
  - Algorithmic enhancements for FDTD
  - Benchmark results
- Application examples
  - 30 GHz KA Band Frontend
  - WiGig Frontend
  - Automotive Radar antennas
- Conclusion

Advanced Numerical Modeling

Today's Design Challenges:

- Design Complexity
- Tight Coupling with other electronics
- Effects of advanced packages
- Varying dimensions/aspect ratios
- User interaction/ environment
- . . .



- Accurate and powerful tools for numerical EM modeling needed

XPU FDTD technology

- ✓ Full 3D FDTD modeling
- ✓ Memory and CPU time efficient

XPU Technology

IMST invented software acceleration technique for FDTD simulation on modern CPU‘s

- ✓ Specific assembler code created for each simulation to fit CPU architecture and simulation model
- ✓ Individual code adaptation for latest CPU’s (AVX, AVX2,…)
- ✓ Speed not limited by RAM access time due to efficient last level cache usage (multiple time step principle)
- ✓ Ability to access the complete RAM of PC (> 512 GB today)
- ✓ High simulation speed for all simulation model sizes
- ✓ Multiple PC’s using the XPU technique can be efficiently clustered
- ✓ Efficient simulation option by swapping on hard disk (simulation size of more then 1 TB possible)

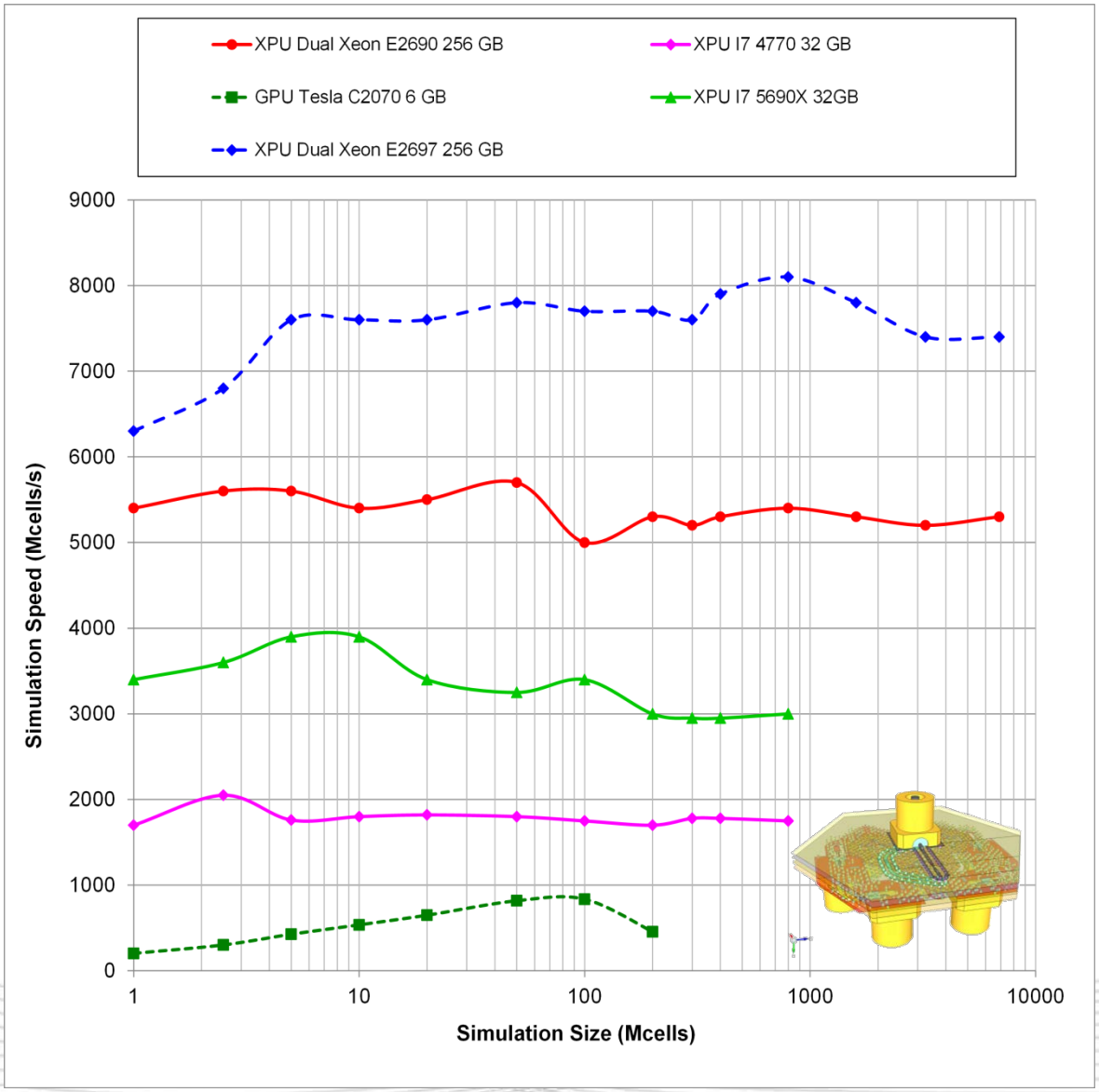
XPU Technology

Evaluation of algorithmic components and resulting performance

	Multi Thread	Multi Time Stepping	E&H	AVX	Speed Mcells/s	
1 core	x	x	x	x	108	← Optimized FDTD code
	x	x	x	√	183	
	x	x	√	√	295	
	x	√	√	√	468	
16 cores	√	√	√	√	5600	← EMPIRE XPU

2 x Intel Xeon E5-2687 W, 3.1 GHz, 16 cores

XPU Technology vs. GPU



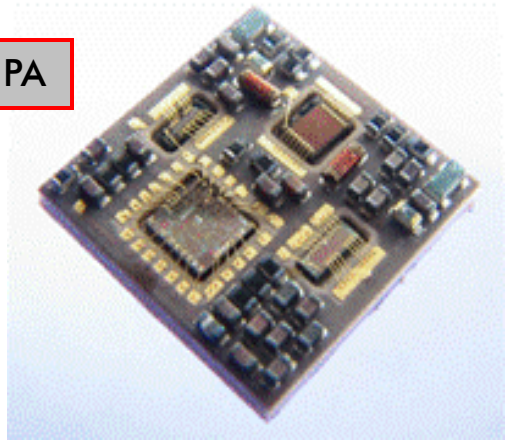
XPU technology surpasses simulation speed of GPU cards for FDTD simulations

Cost- & Energy- efficient computing

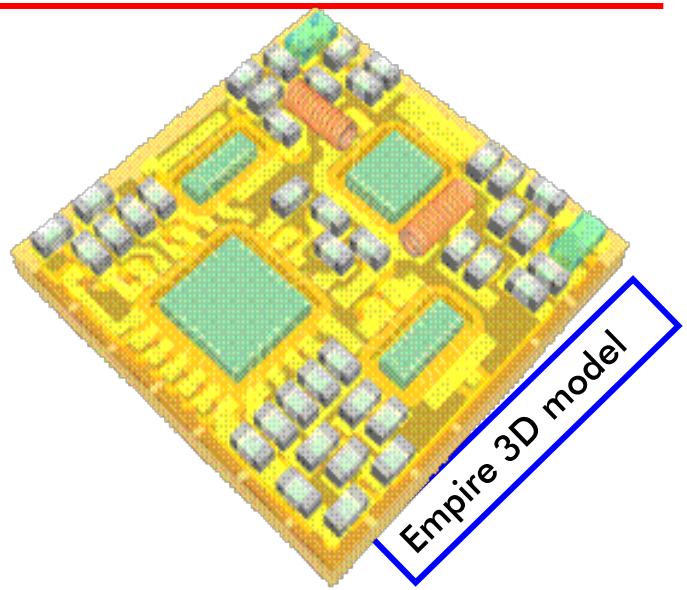
I7-4770 PC	~ 700 €
I7-5960x PC	~ 1800 €
Dual Xeon workstation	~ 7000 €
Workstation + GPU	~ 9000 €

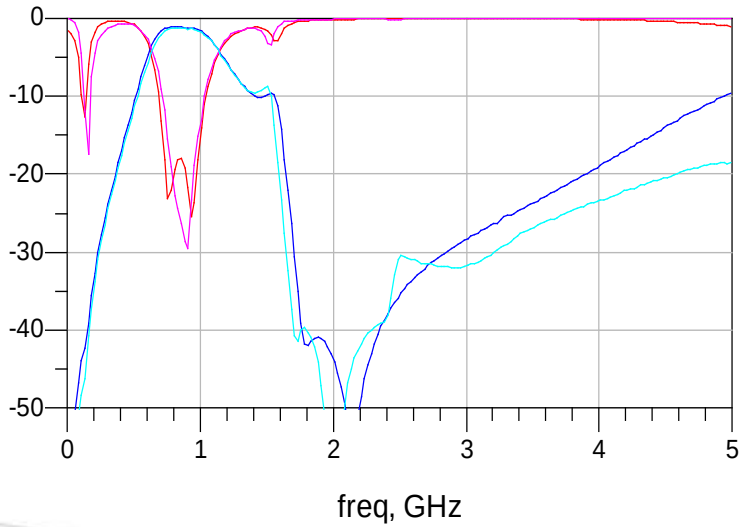
Complete Mobile Phone: PA analysis

Photo of PA



Complete HPA module for GSM and XCS



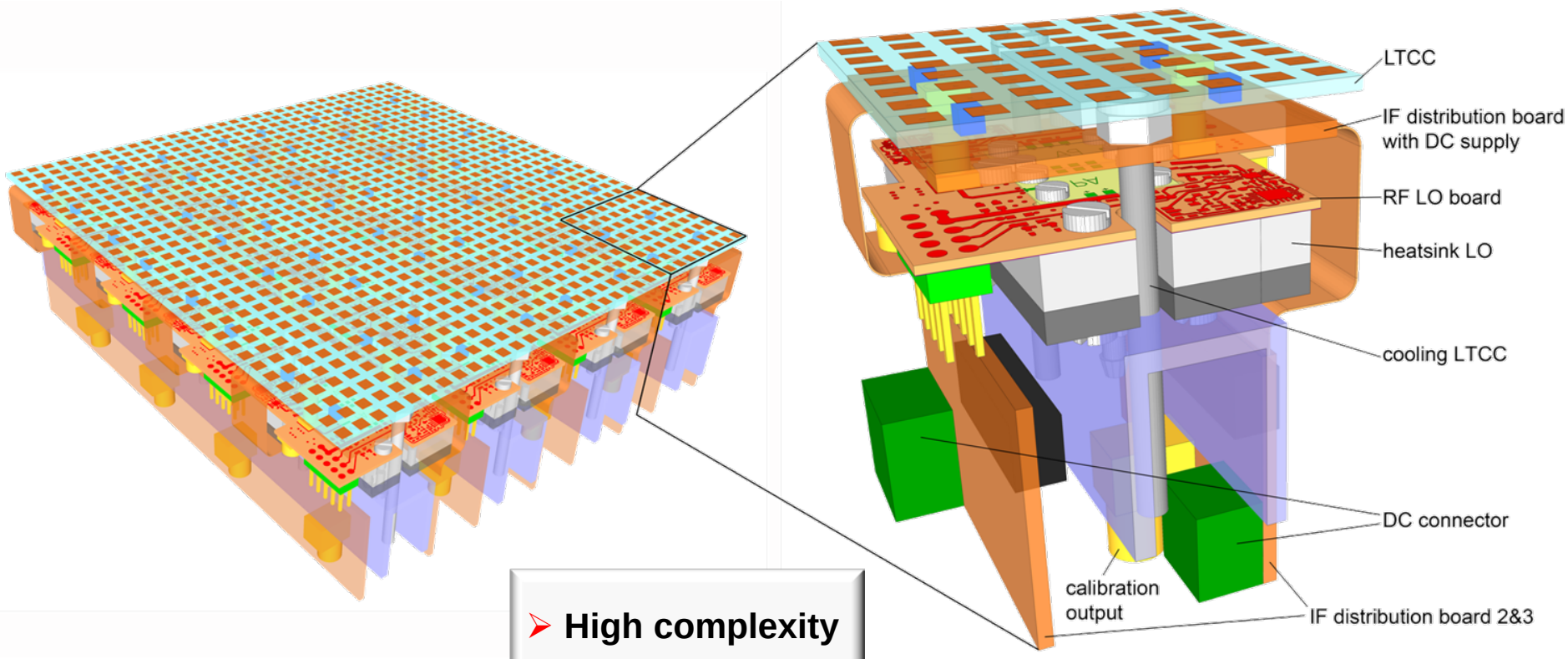


Output matching GSM:simulation vs. measurement

- Frequency DC - 5 GHz
- Resolution: 25 µm
- 32 ports
- Simulation time: 1 min/port (3 Mcells, 150 MByte RAM)
- 3D EM simulation includes all couplings

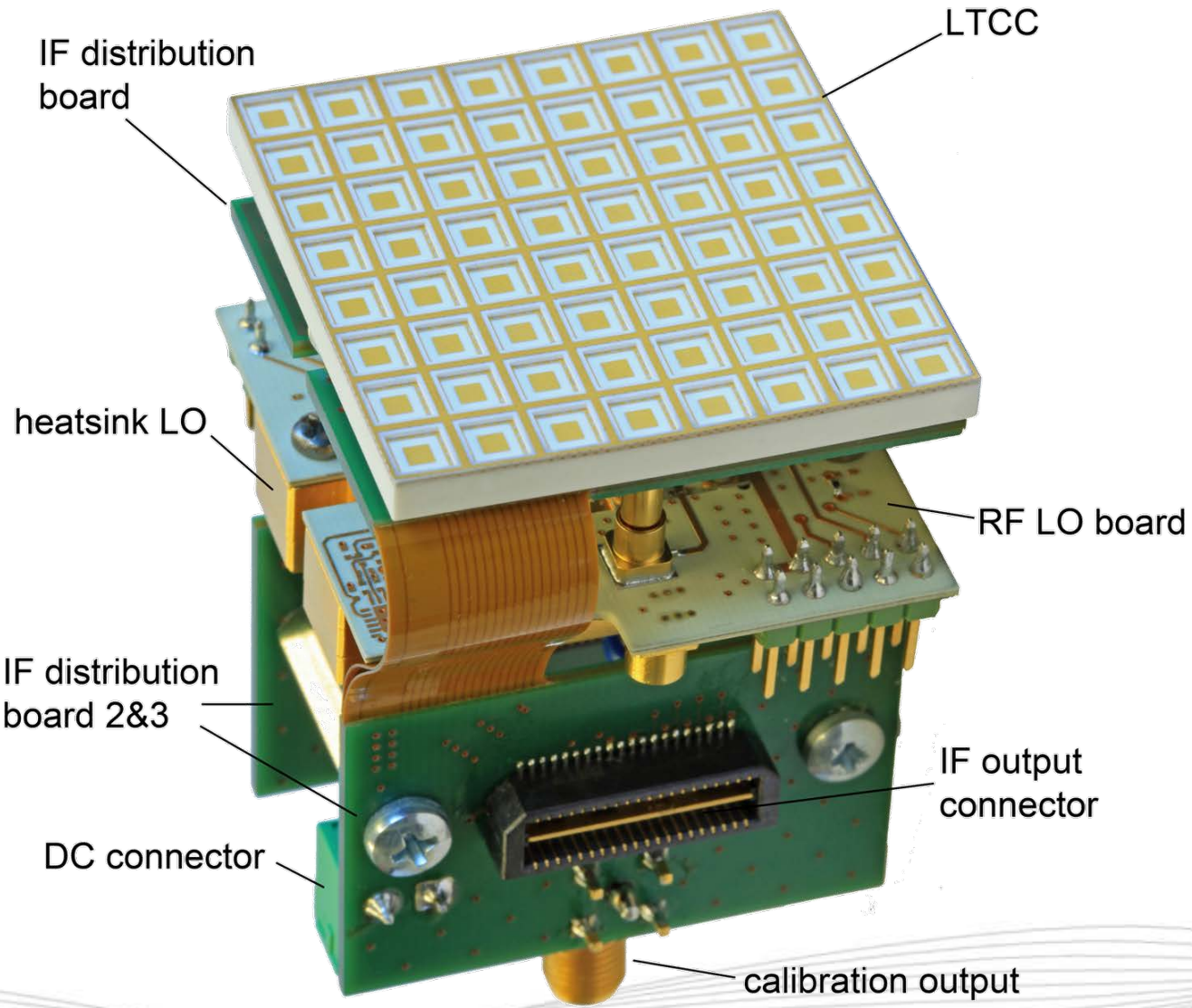
KA-Band / 5G DBF frontend module

Flexible modular concept

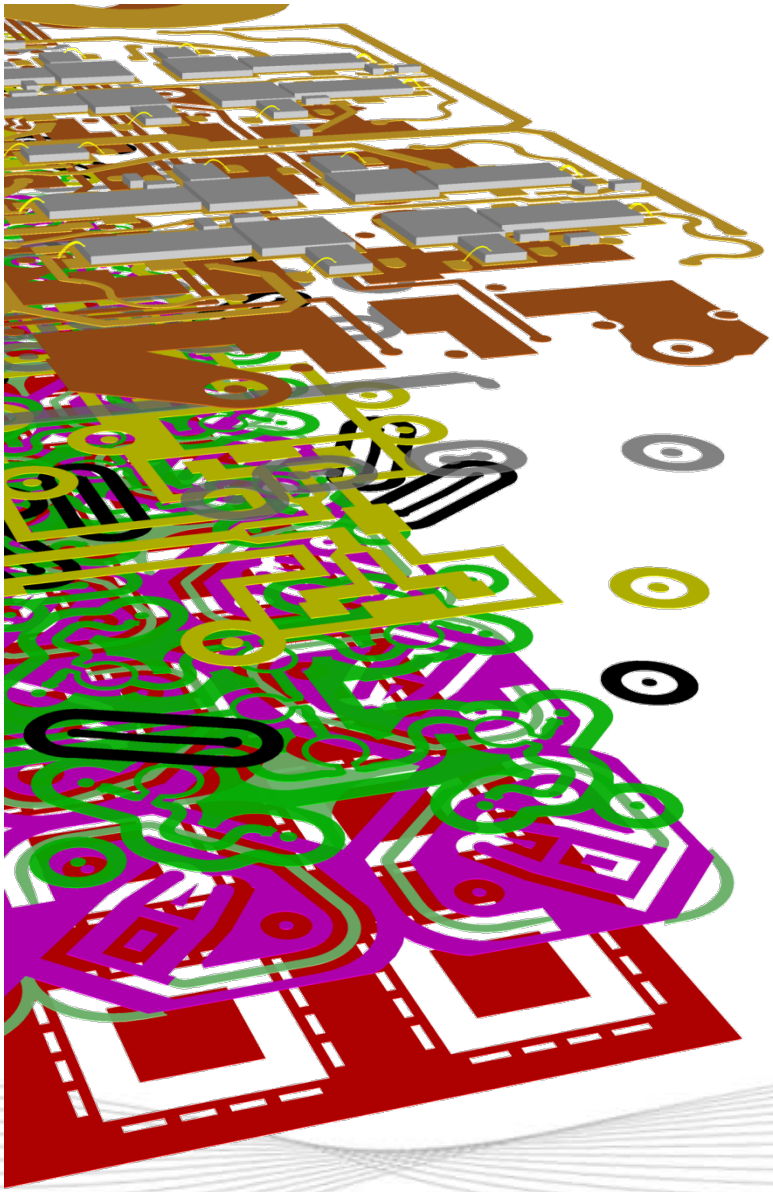


- **High complexity**
- **High flexibility**

KA-Band / 5G DFB TX frontend module



LTCC frontend: Main functional layers



RF chipsets, interconnects

IF network

DC network

LO network

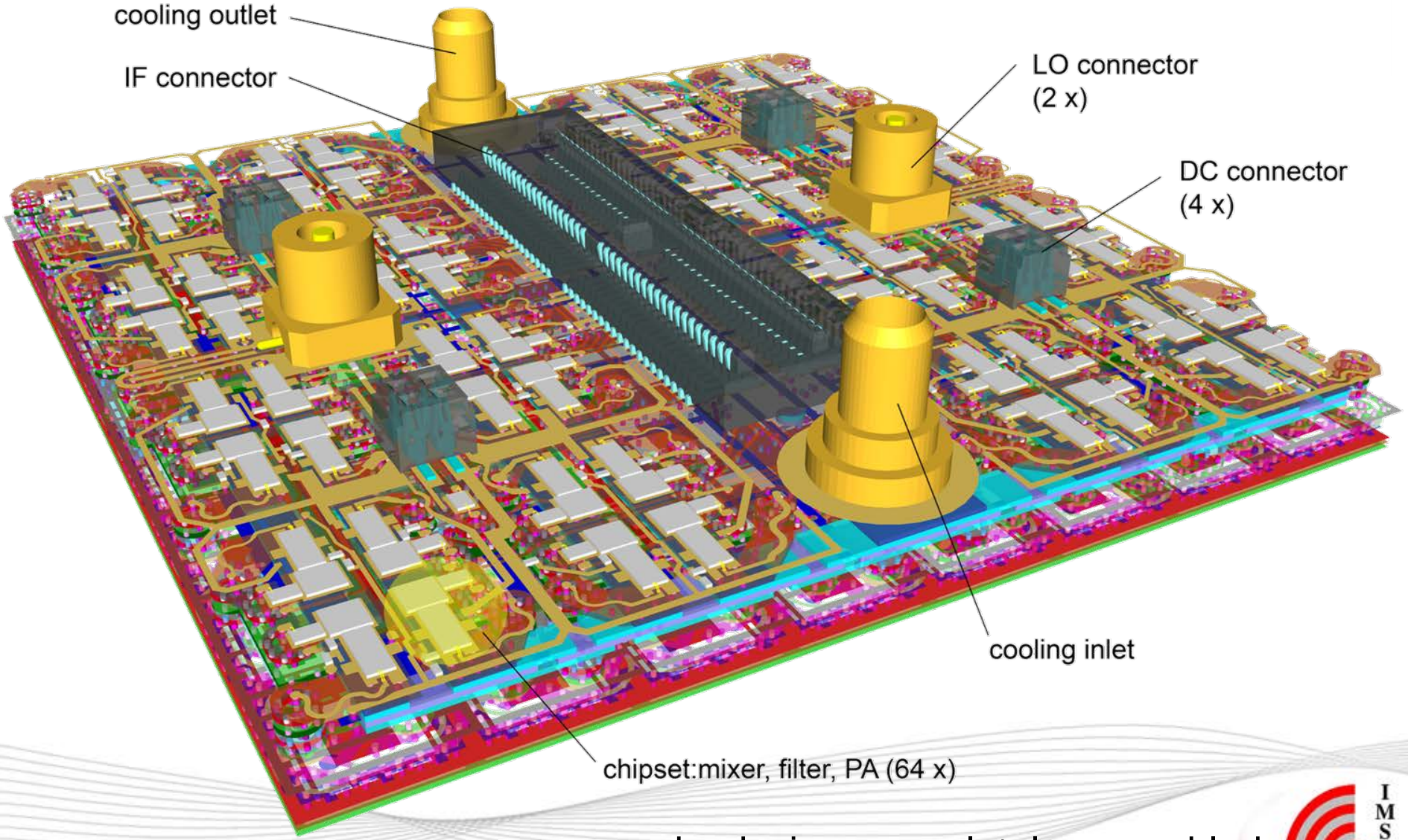
interconnect RF-antenna

calibration network

90° hybrid circuits

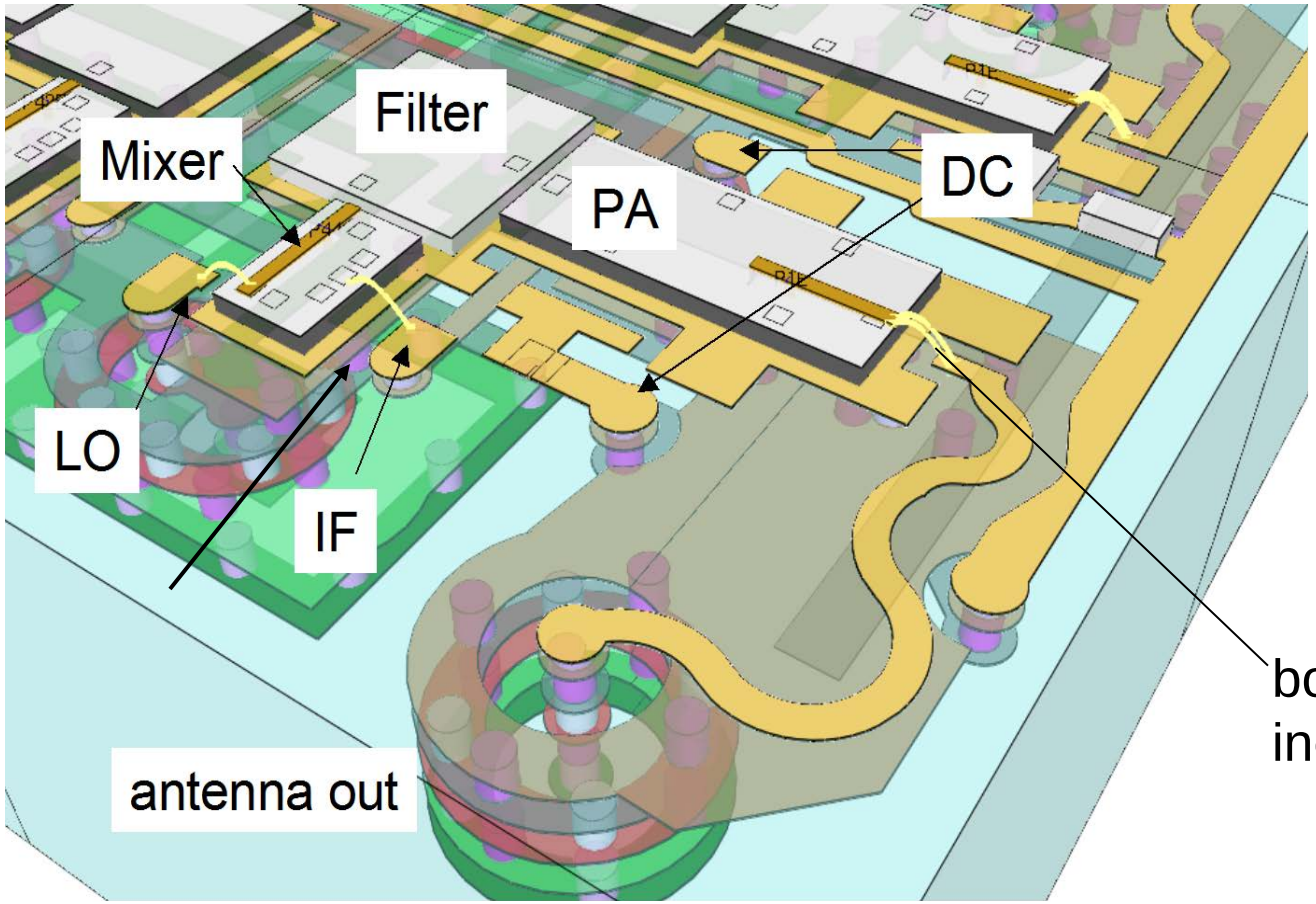
antenna elements

LTCC frontend: RF circuitry architecture



back view, completely assembled

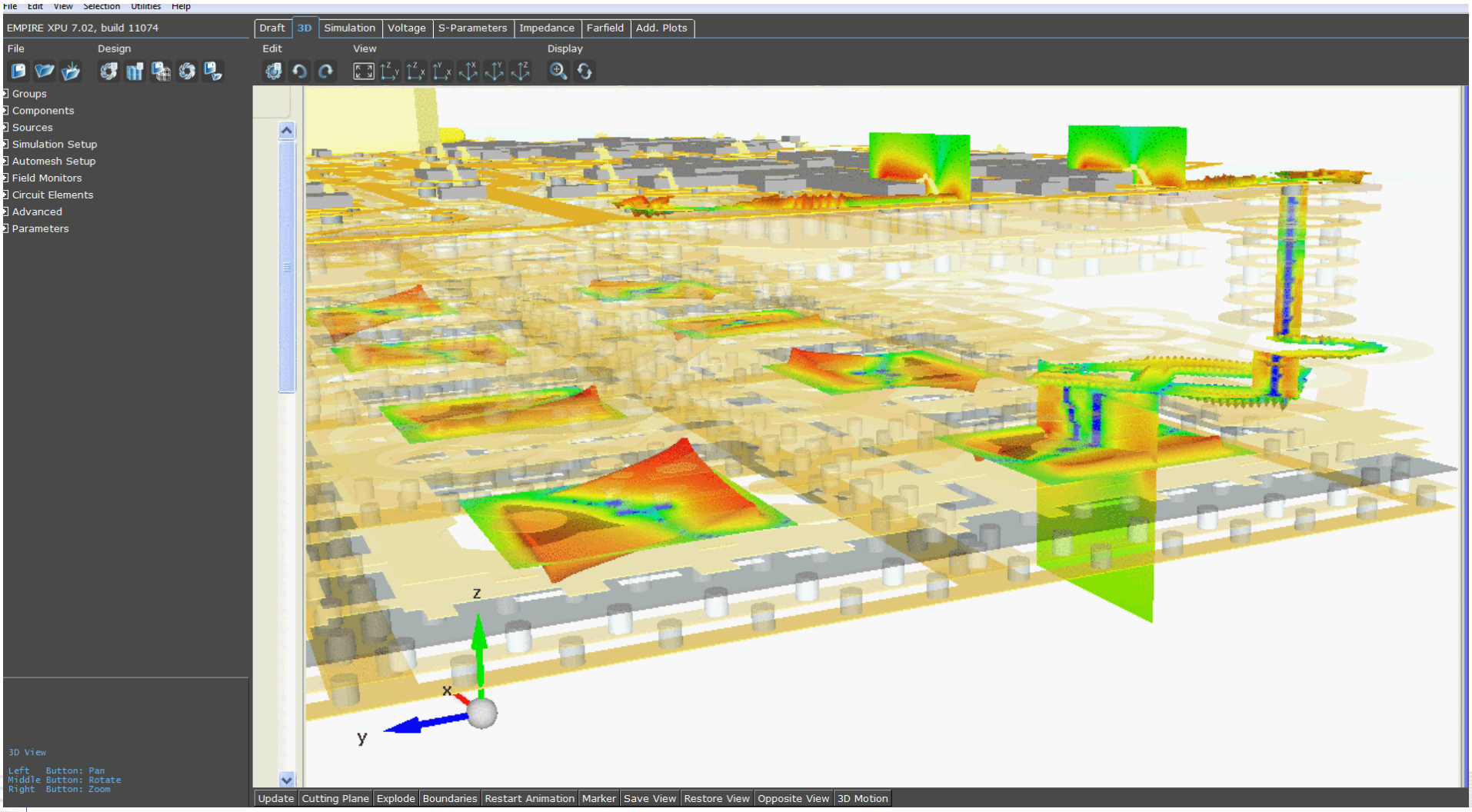
LTCC frontend: RF chipset



- **mixer combines 870 MHz IF and 30.6 GHz LO**
- **PA Output power ~ 10 dBm**

bond wires
included in simulation

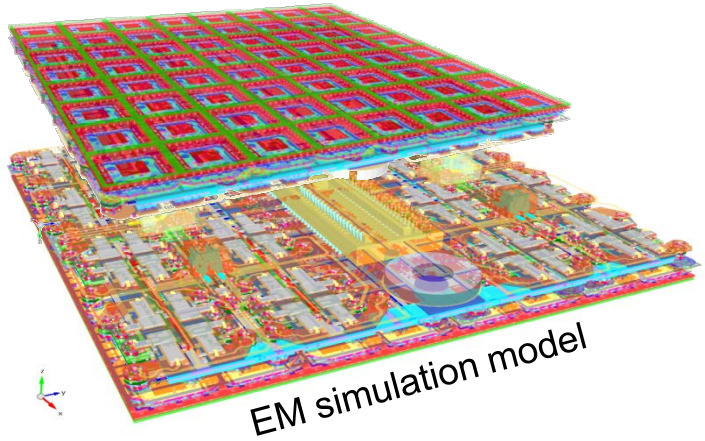
30 GHz KA Band frontend

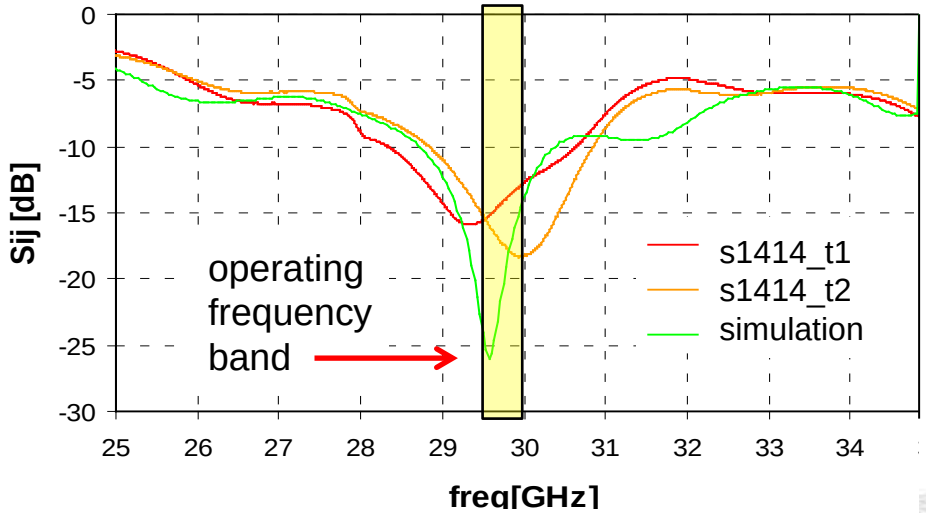


30 GHz KA Band frontend

RF Frontend incl. 8x8 array antenna

- simulation on dual Xeon E5-2697
- 600 Million cells (1664x1650x225)
- grid: 10 µm < Δ < 215 µm
- 56000 objects
- memory usage: Field 16 GB
- simulation Speed: ~ 5800 Mcells/s
- simulation Time: < 2h *

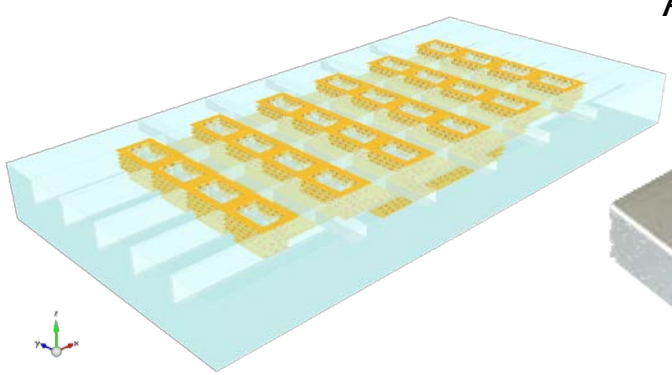




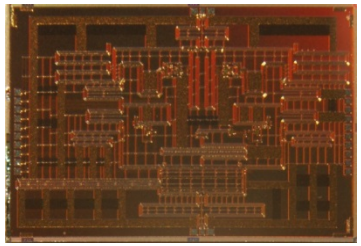
Measurement and simulation results

* simulation on Dual Xeon E5-2697 workstation

60 GHz WiGiG Frontend Module



Antenna



SiGe chip design

- Size: 80 mm x 170 mm
- 60 GHz Substrate Integrated Waveguide Array Antenna in LTCC
- Operating frequency: 57-63 GHz (10 %)
- Max. scanning range: ± 30° in one plane
- Total array gain: 18-20 dBi

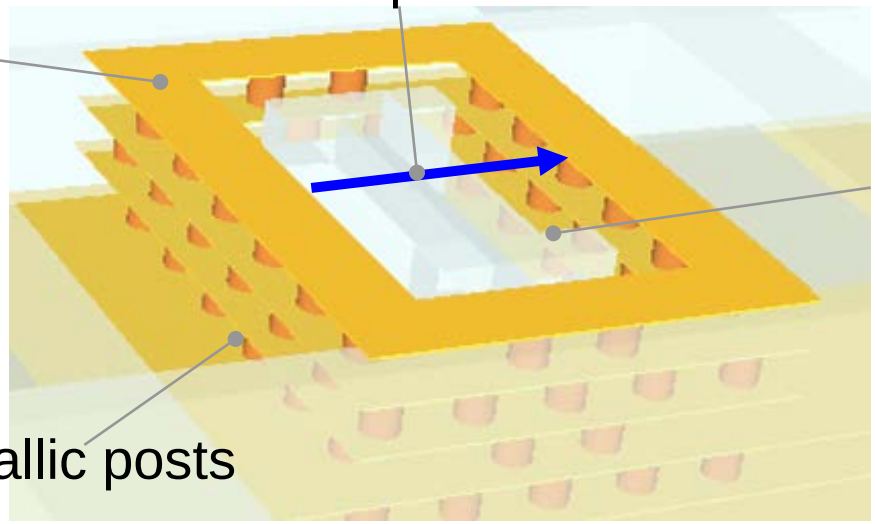
Antenna Element Realization Technique

(SIW) Substrate Integrated Waveguide in Low Temperature Co-fired Ceramic *(LTCC)*

Leakage through via gaps
Band stop structure

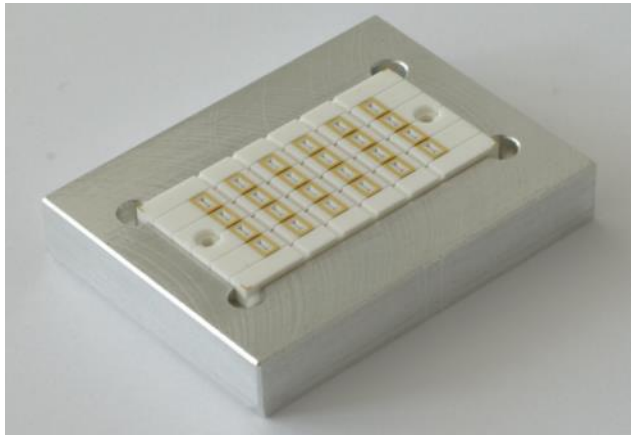
High number of layers
Large number of vias

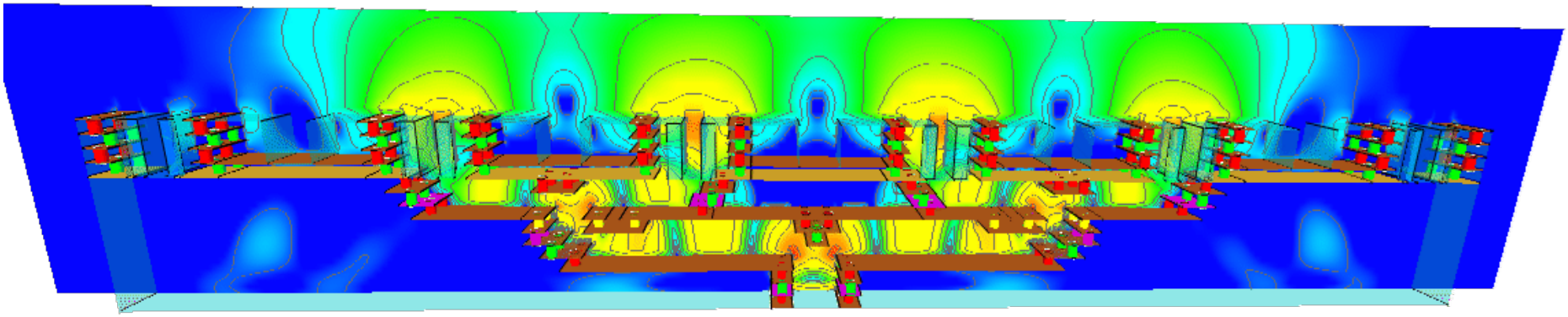
High ε_r



60 GHz WiGig Frontend Module

- size: 80 mm x 170 mm
- mesh: 35 Million cells
- resolution 25 µm < d < 250 µm
- memory usage: 1.5 GB
- simulation speed: 5200 Mcells/s
- simulation time: 1 min*

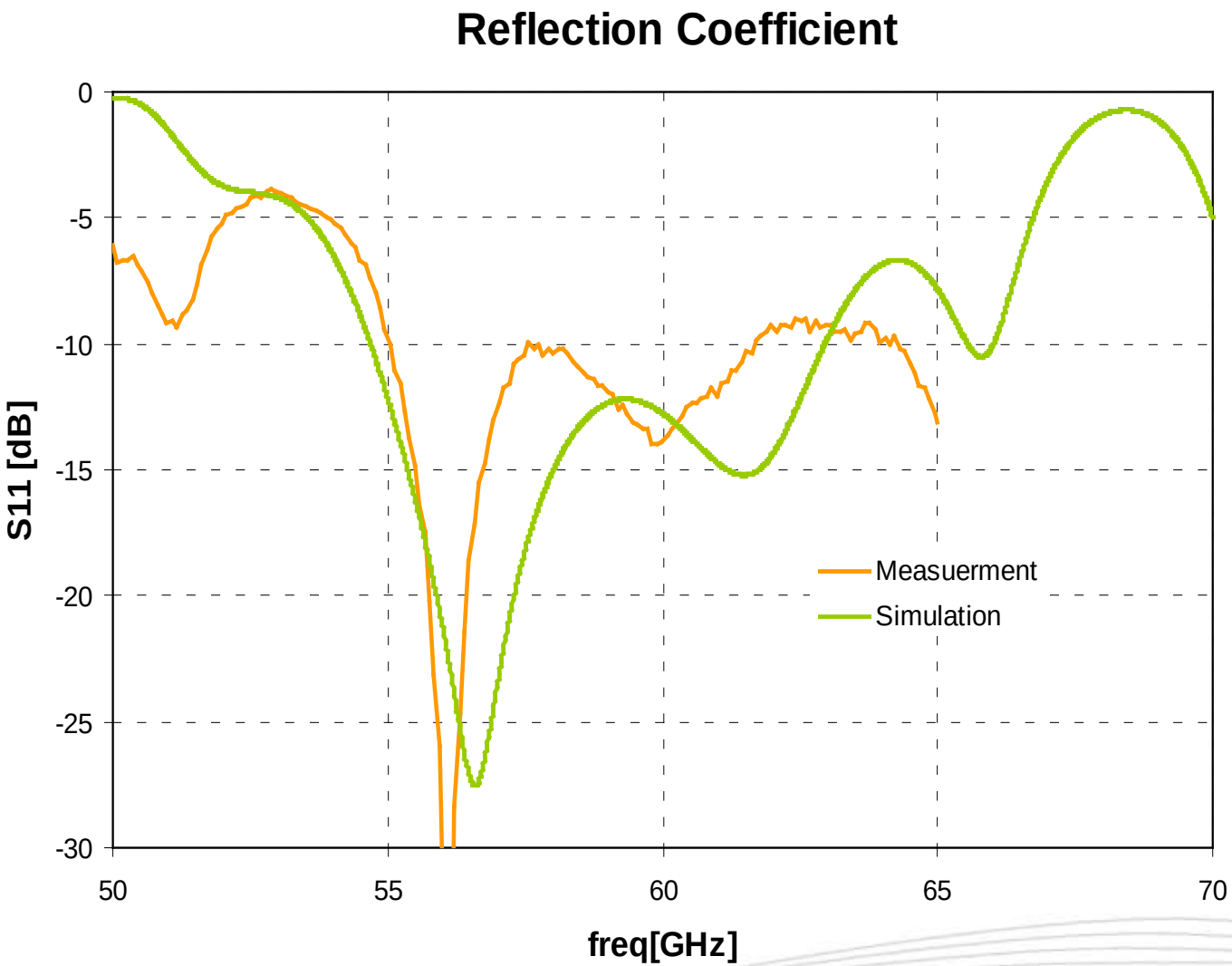




Electric field @ 60 GHz

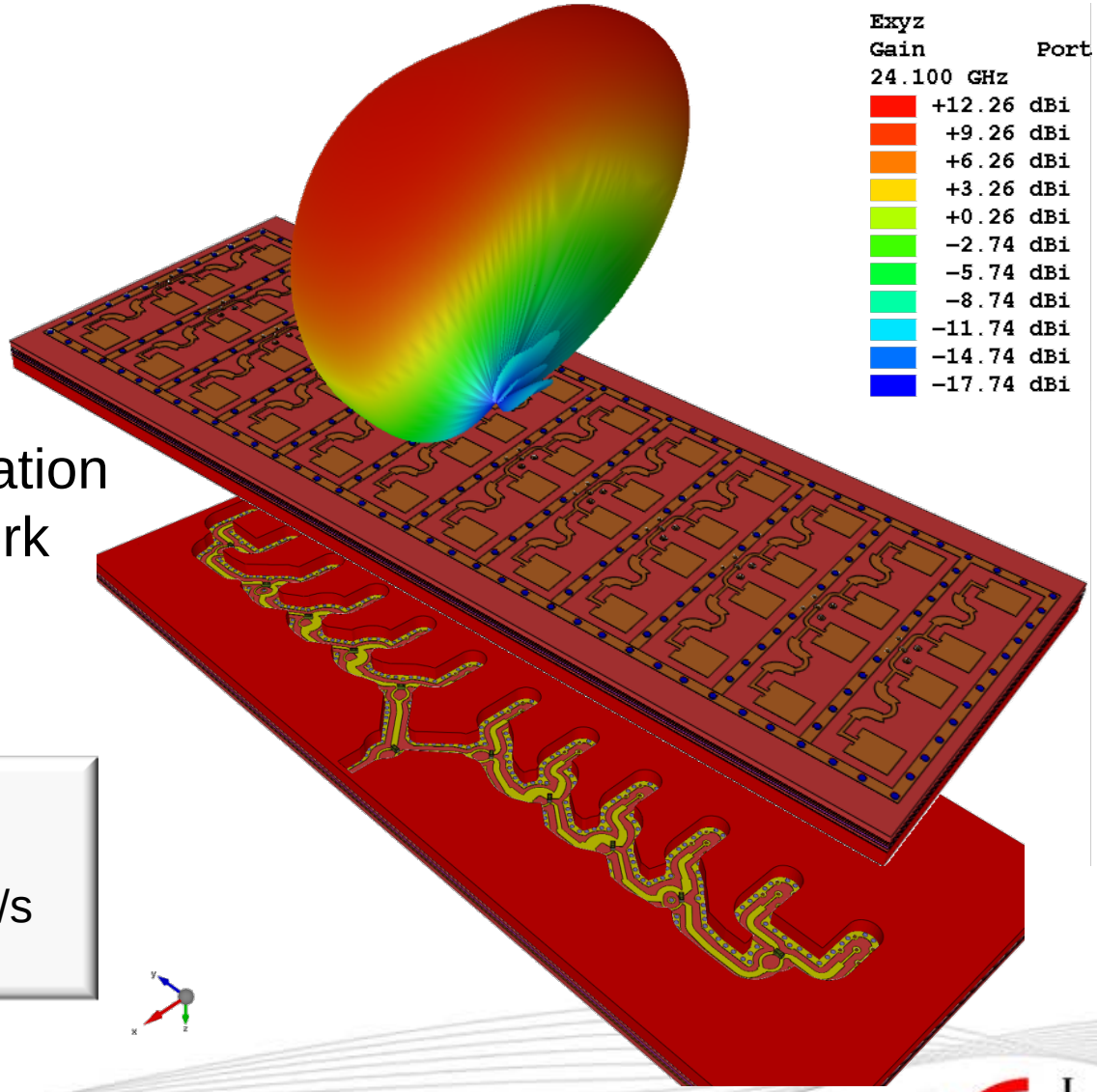
* simulation on Dual Xeon E5-2697 workstation

60 GHz WiGiG Frontend Module



24 GHz radar antenna (TX)

- 4 x 12 element array
- Backside microstrip feed network with Wilkinson dividers
- Accurate 3D EM simulation of antenna, feed network and backside casing

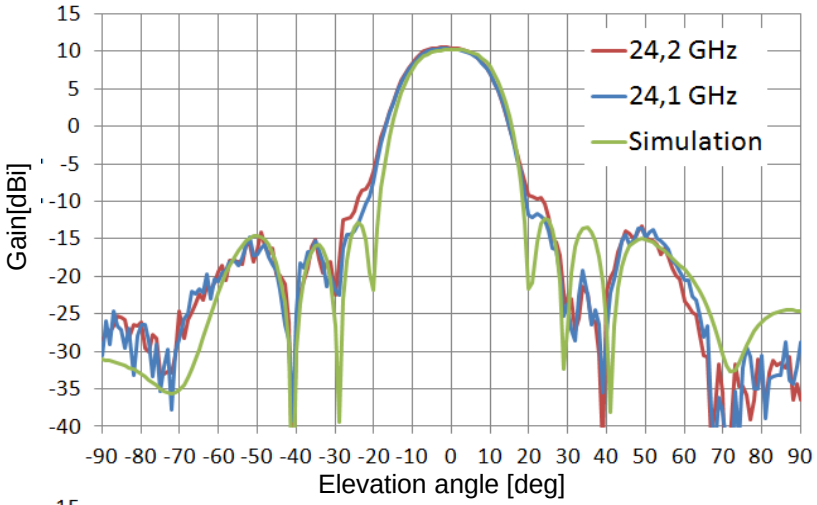


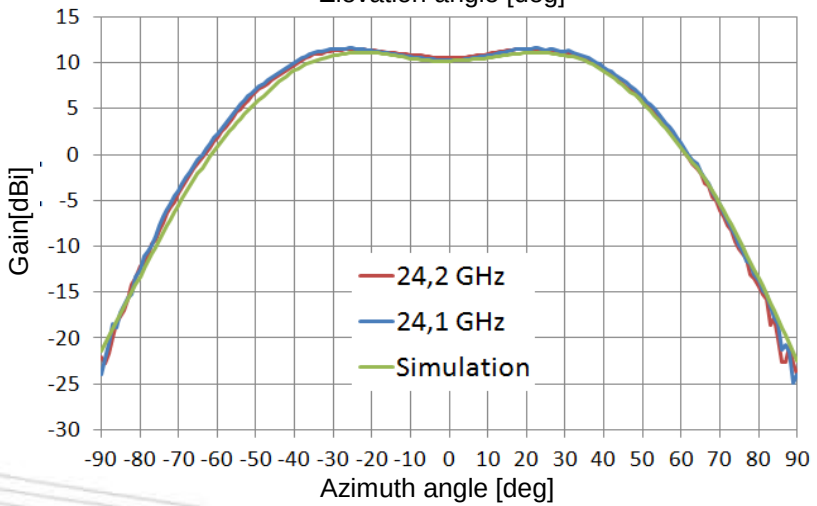
- 20 GHz – 28 GHz
- 53 Million cells, ~ 2 GB
- simulation speed: 7000 Mcells/s
- simulation time: ~8 min*

* simulation on Dual Xeon E5-2697 workstation incl. metal & dielectric loss

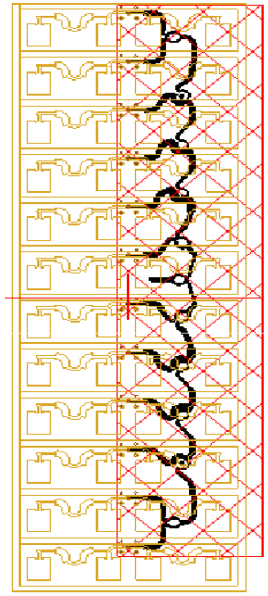
24 GHz radar antenna (TX)

TX antenna measurements





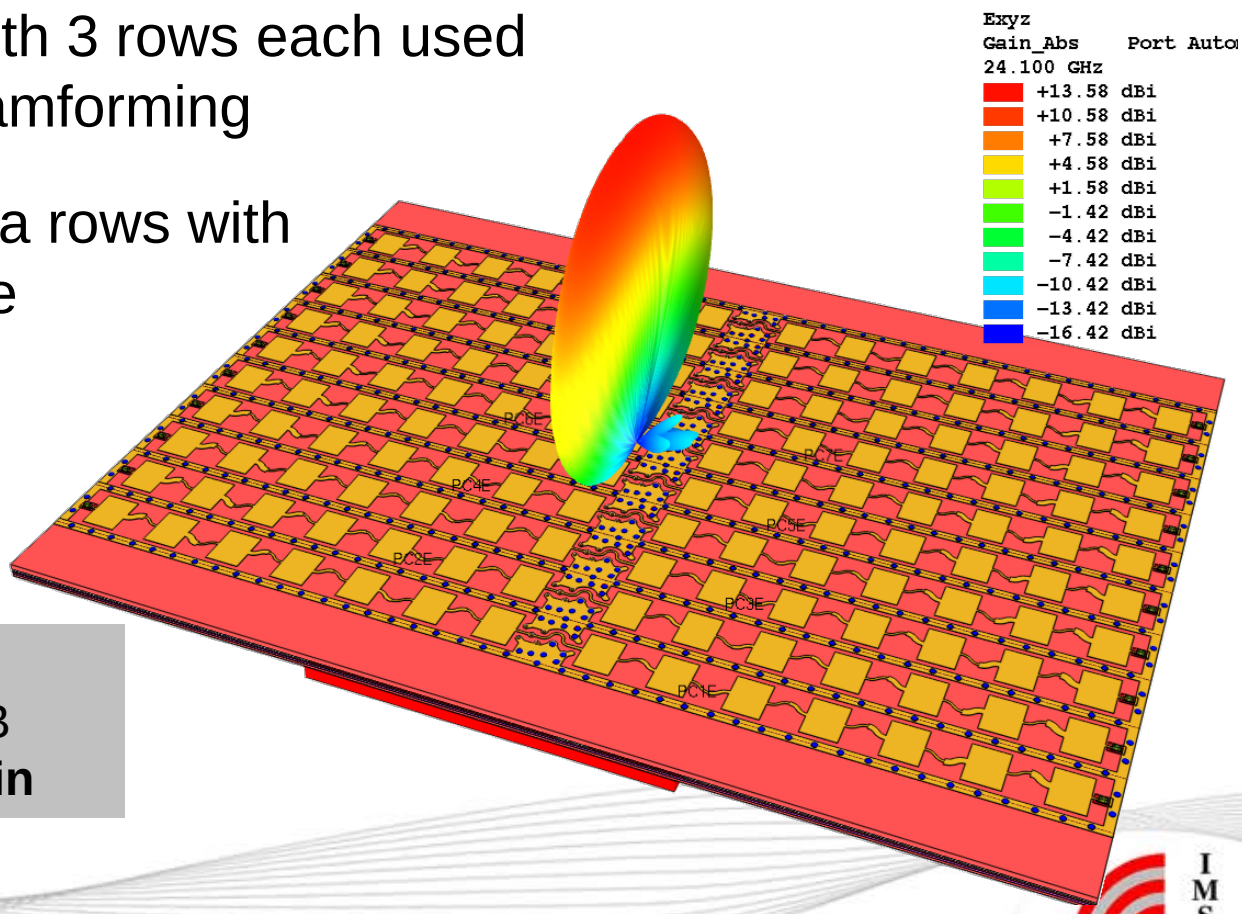
Tx



- ✓ Excellent agreement between measurement and simulation
- ✓ Gain, SLL and elevation as required

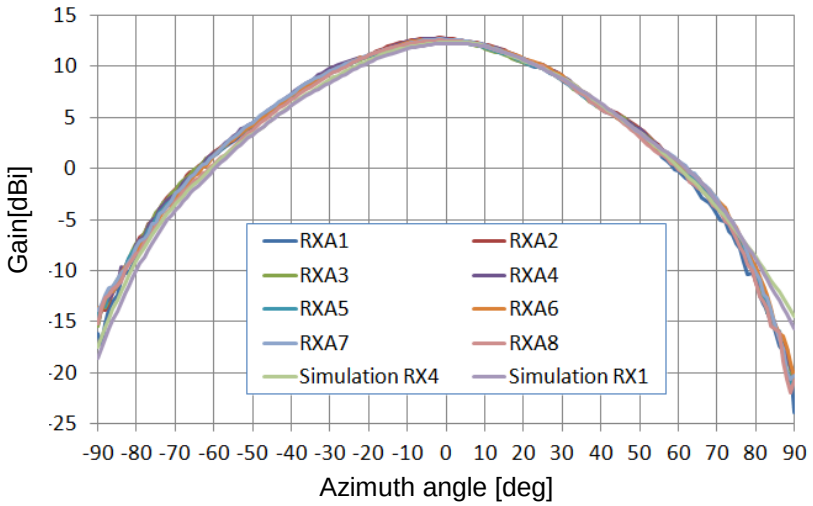
24 GHz radar antenna (RX)

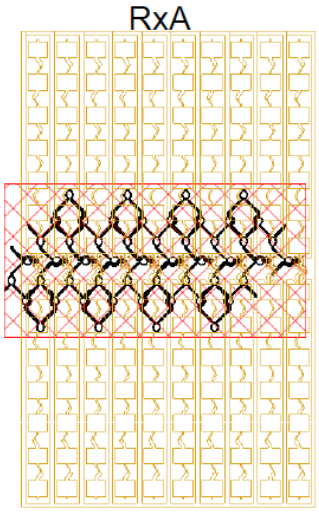
- 10 antenna rows with 14 series fed patch elements in each row
- Eight sub arrays with 3 rows each used for RX azimuth beamforming
- Dual use of antenna rows with innovative backside feed network

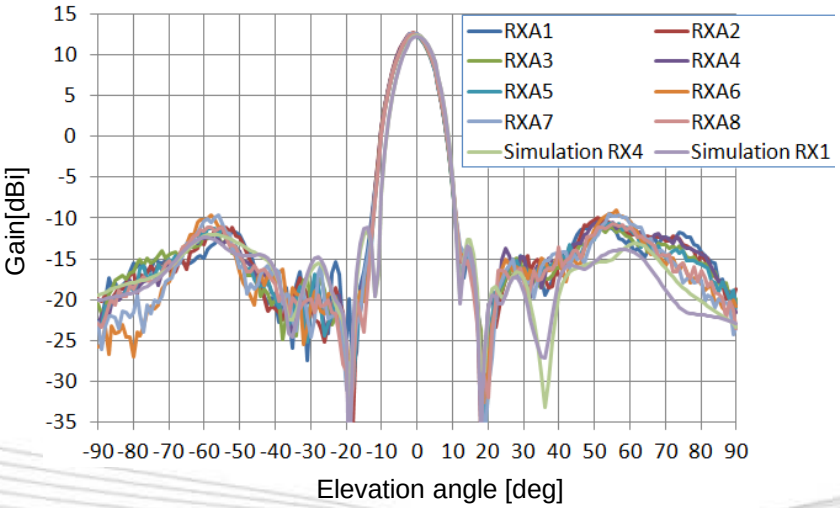


- 20 GHz – 28 GHz
- 216 Million cells, ~ 6.8 GB
- **Simulation time: ~ 25 min**

24 GHz radar antenna (RX)



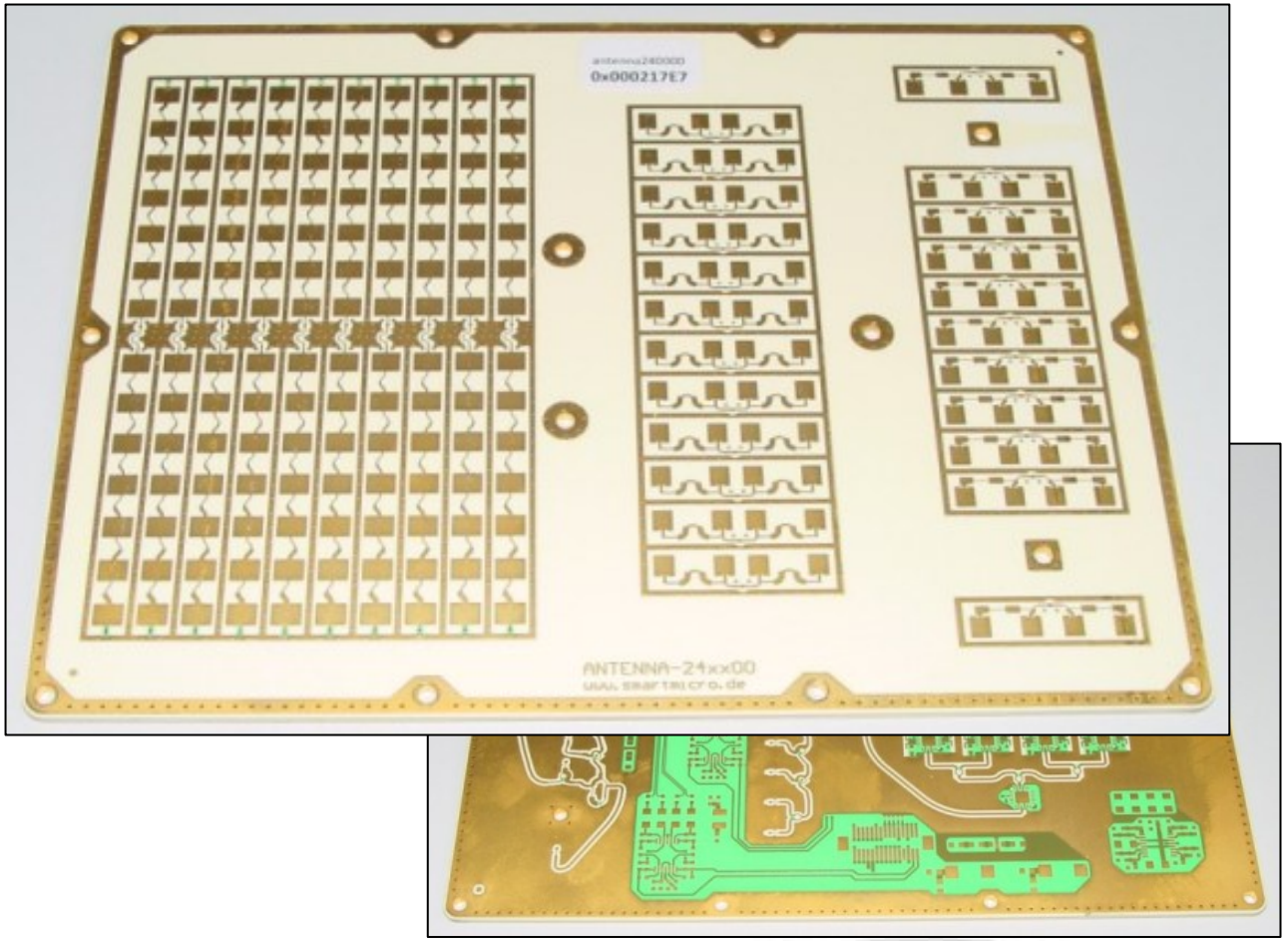




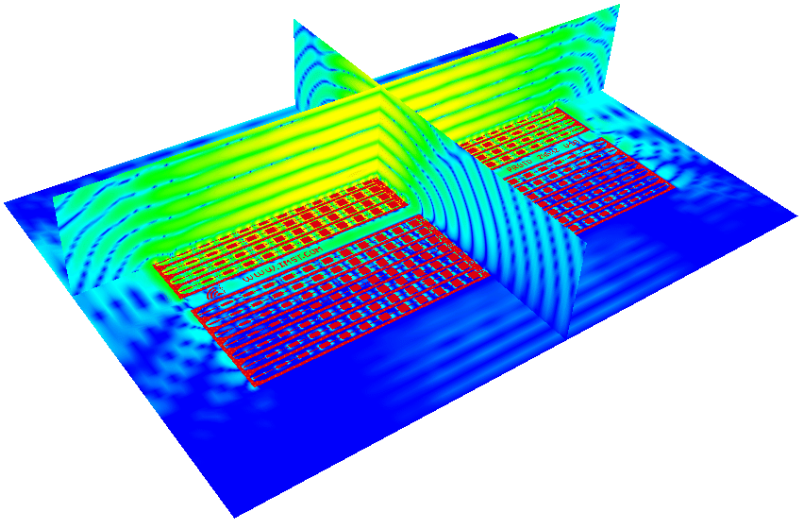
- Gain RX azimuth antenna 1-8
  - Excellent agreement between measurement and simulation
  - Excellent element match
  - Wide azimuth diagram for DBF
  - Good uniform linear array

24 GHz radar TX/RX module

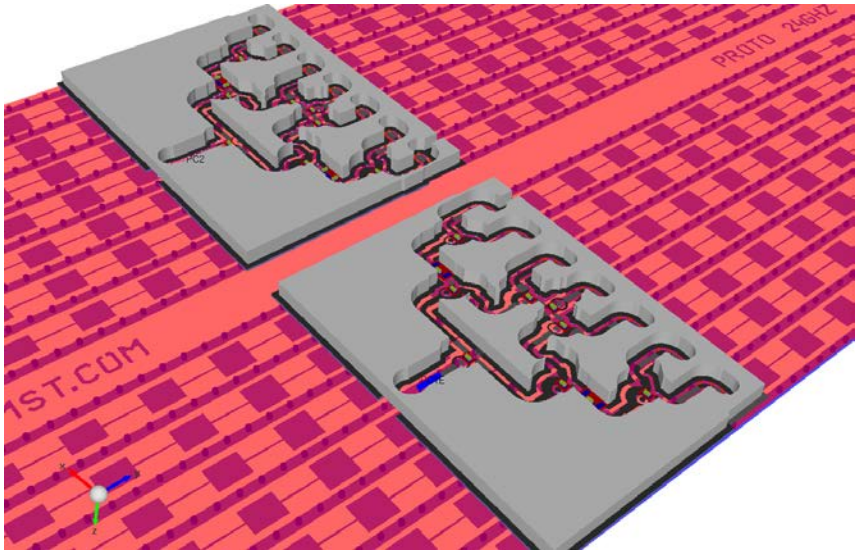
- Manufacturing on Rogers 4350
- 1st shot successful



24 GHz Automotive TX/RX radar antenna



Antenna with near field at 24 GHz

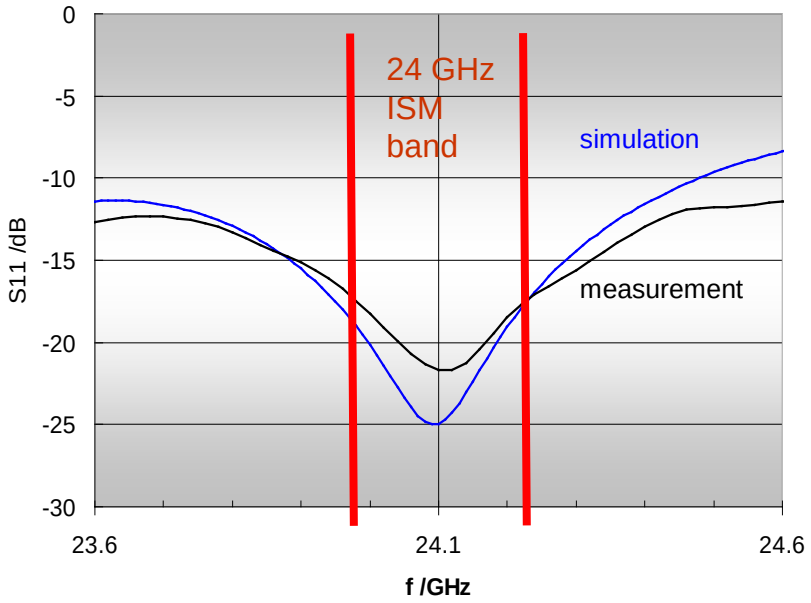


Backside feed network with housing

- size: 80 mm x 170 mm
- dielectric thickness ~ 1mm, 4 metal layers
- 0201 SMD resistors for Wilkinson dividers and antenna rows end load
- 7 x 24 patches for TX & RX
- mesh 1112 x 1300 x 55 cells (108 Million cells)
- resolution 25 µm < d < 500 µm
- memory usage 3.14 GB
- simulation time 7 min (Dual Xeon workstation) ; speed 5850 Mcells/s

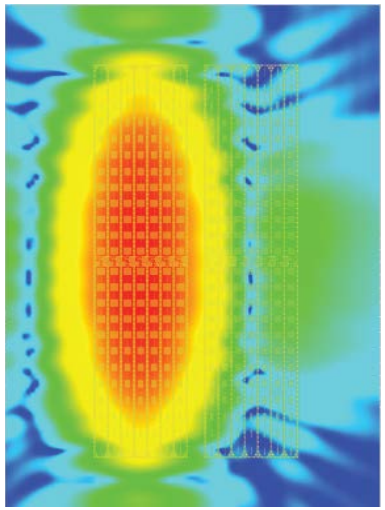
24 GHz Automotive TX/RX radar antenna

Return loss

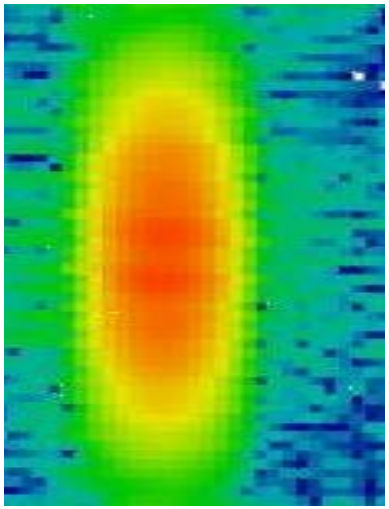


Nearfield – comparison simulation/measurement

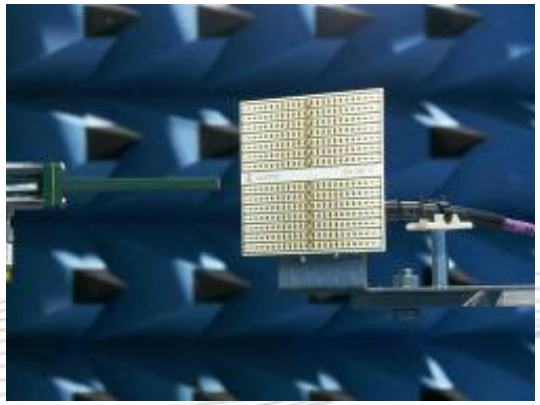
simulation



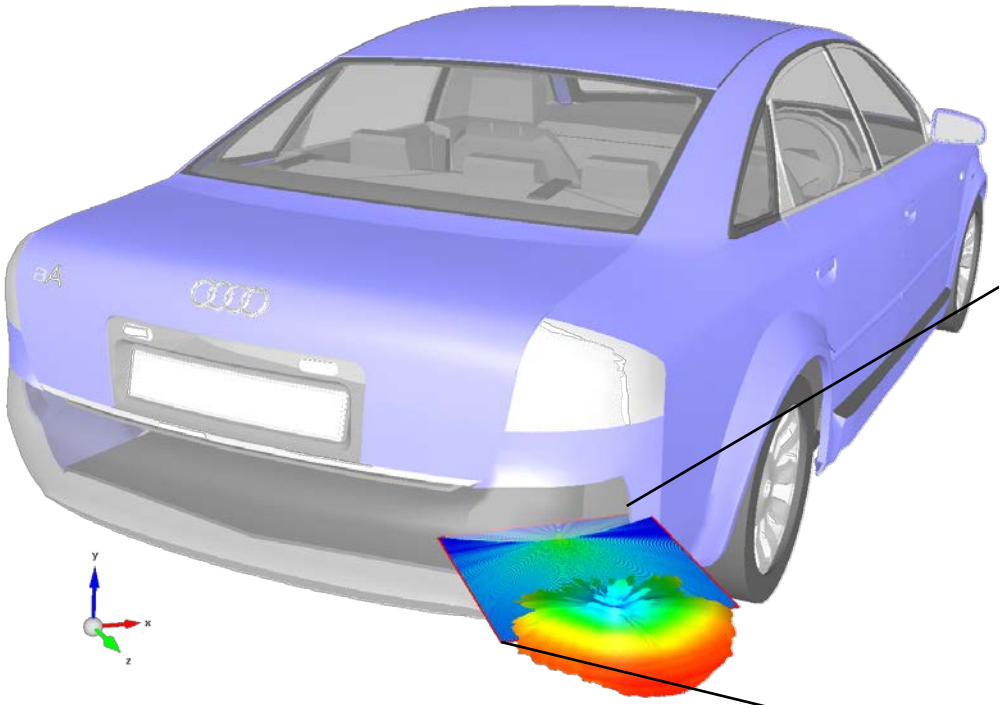
measurement



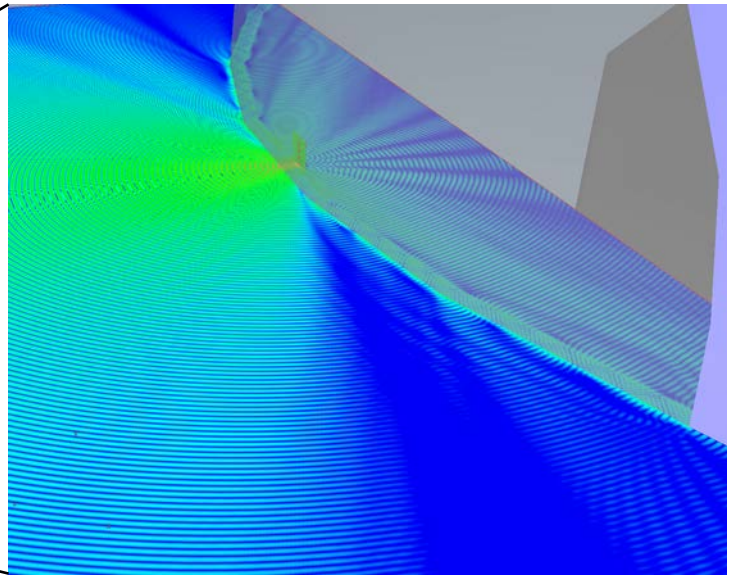
- good agreement between measurement and simulation



77 GHz radar antenna



Farfield & Electric field strengths at
f = 77 GHz



- frequency: DC - 77 GHz
- all parts metal except windscreen, bumper and tire (dielectric)
- results: s11, 2D & 3D farfield, nearfield in cutplanes
- size: 400 Million FDTD cells, 10 GB memory
- simulation speed: 6200 Million cells/s Simulation time: 20 min*

* simulation on Dual Xeon E5-2697 workstation

Conclusion

- ✓ Innovative FDTD coding utilizing XPU technology enables fast parallel computation on multicore and multi CPU workstations in a memory efficient way
- ✓ The XPU technique can utilize the full memory of the PC to simulate large & complex EM-models
- ✓ Empire shows accurate simulation results within very short simulation time for complex frontend designs
- ✓ The high accuracy of the simulation results enables shorter prototype cycles and hence development costs are reduced

