INSA INSTITUT NATIONAL DES SCIENCES APPLIQUÉES TOULOUSE

DEPARTEMENT DE GENIE ELECTRIQUE ET INFORMATIQUE

AFCEM

Microwave & RF

IC-EMC
Simulation of Electromagnetic Compatibility of Integrated Circuits

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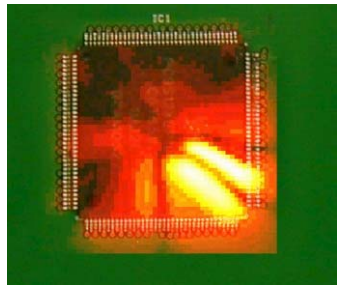
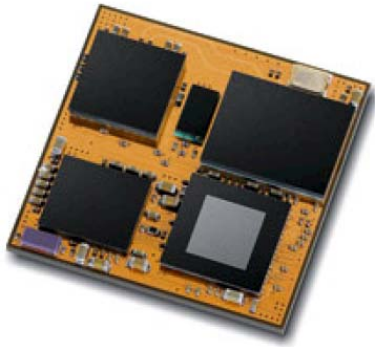
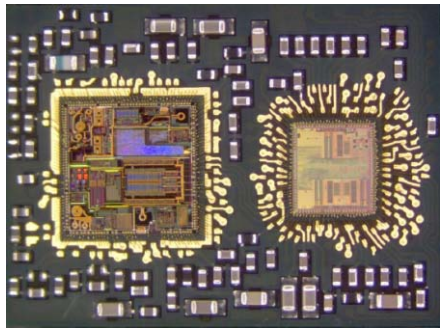
CONTENTS

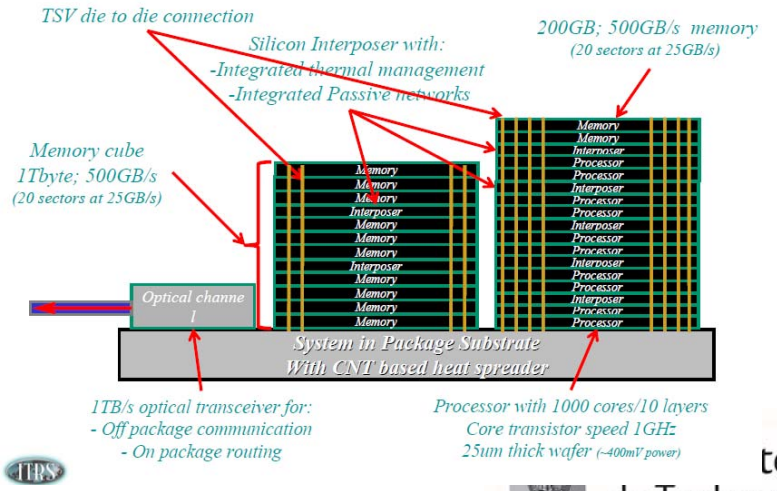
CONTEXT - WHY EMC OF IC ?

- Until mid 90's, IC designers had no consideration about EMC problems in their design..
- Starting 1996, automotive customers started to select ICs on EMC criteria
- Starting 2005, mobile industry required EMC in System in package
- Starting 2015, massive 3D integration will require careful EMC design
- "Urgent Need to Integrate EMC and Product Safety into Engineering Curriculum of Technical Universities"





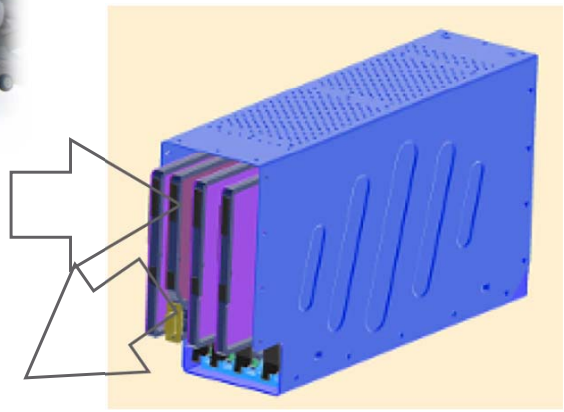




CONTEXT - FROM SYSTEM TO INTEGRATED CIRCUIT EMC

- **Susceptibility**

Equipment



Radar

Boards

Components

Hardware fault
Software failure
Function Loss

- **Emission**

Personal Devices

Safety systems

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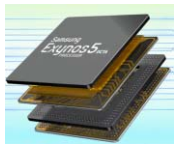
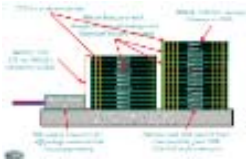
TECHNOLOGY TRENDS TOWARDS TERA DEVICES

Today

	2004	2007	2010	2013	2016	2020
Technology	130nm	90nm	45nm	28nm	14nm	5nm
Complexity	250M	500M	2G	7G	15G	150 G
Packaging						
Mobile generation	3G 	3G+ 	4G 	4G+ 	5G 	
Embedded blocks	Core DSPs 10 Mb Mem	Dual core Dual DSP RF Graphic Process. 100 Mb Mem Sensors	Quad Core Quad DSP 3D Image Proc Crypto processor Reconf FPGA, Multi RF 1 Gb Memories Multi-sensors	Octa Core Multi DSP 3D 4K Image Proc Crypto, sensor, position processor Agregated RF 2 Gb Memories		?

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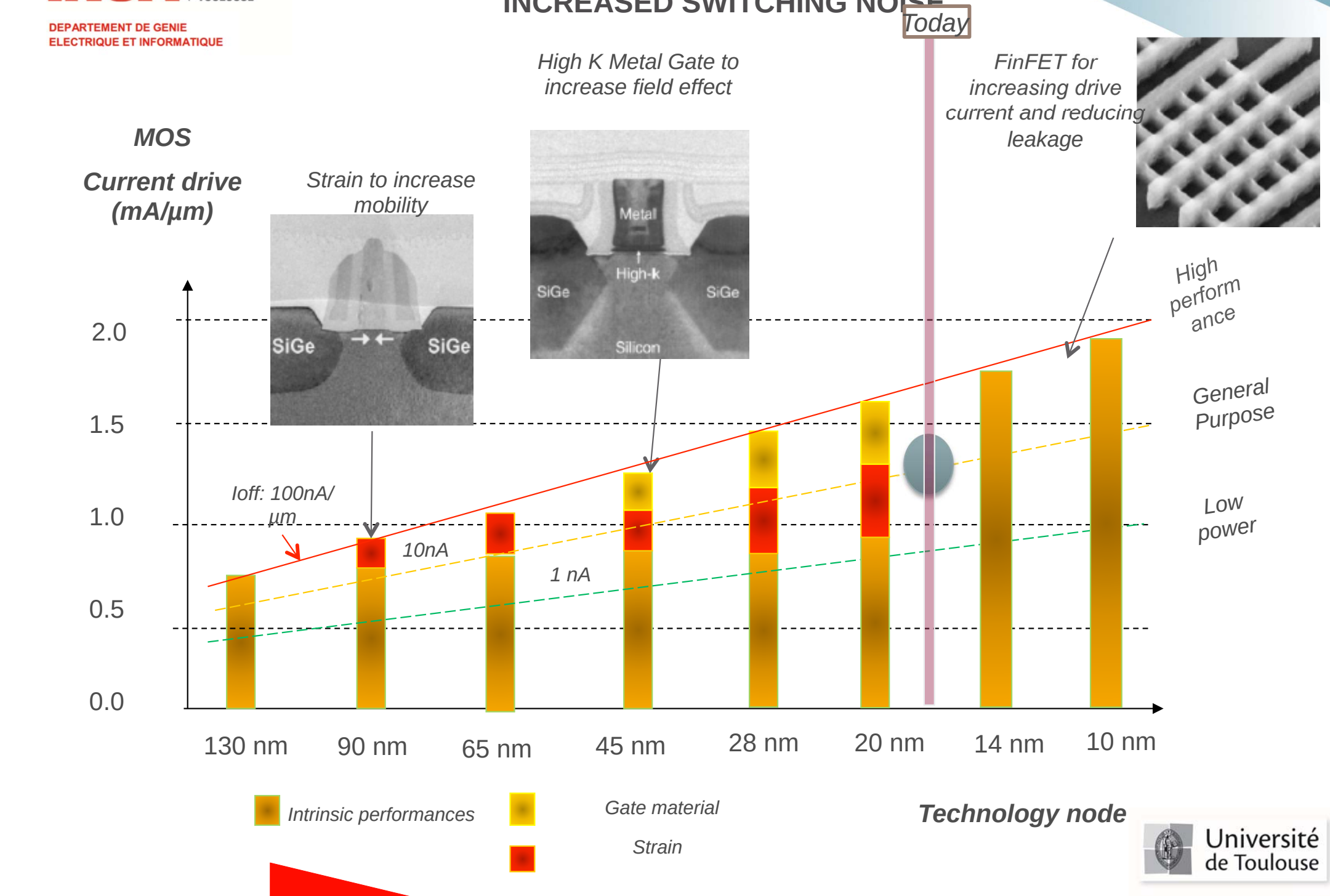
TECHNOLOGY TRENDS
INCREASED SWITCHING NOISE



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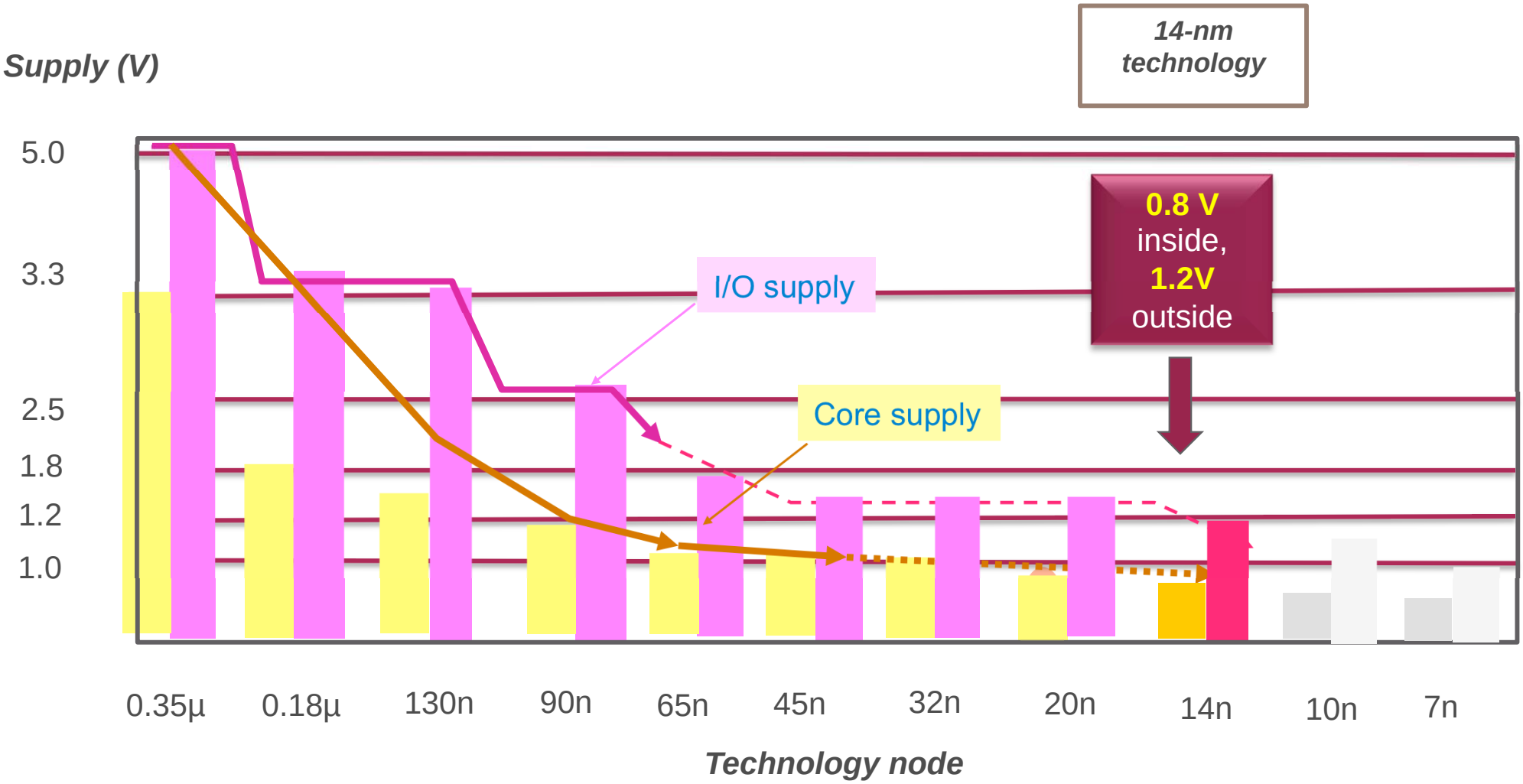
TECHNOLOGY TRENDS
DECREASED NOISE MARGIN

- VDD is lowered to 800mV in 14-nm technology

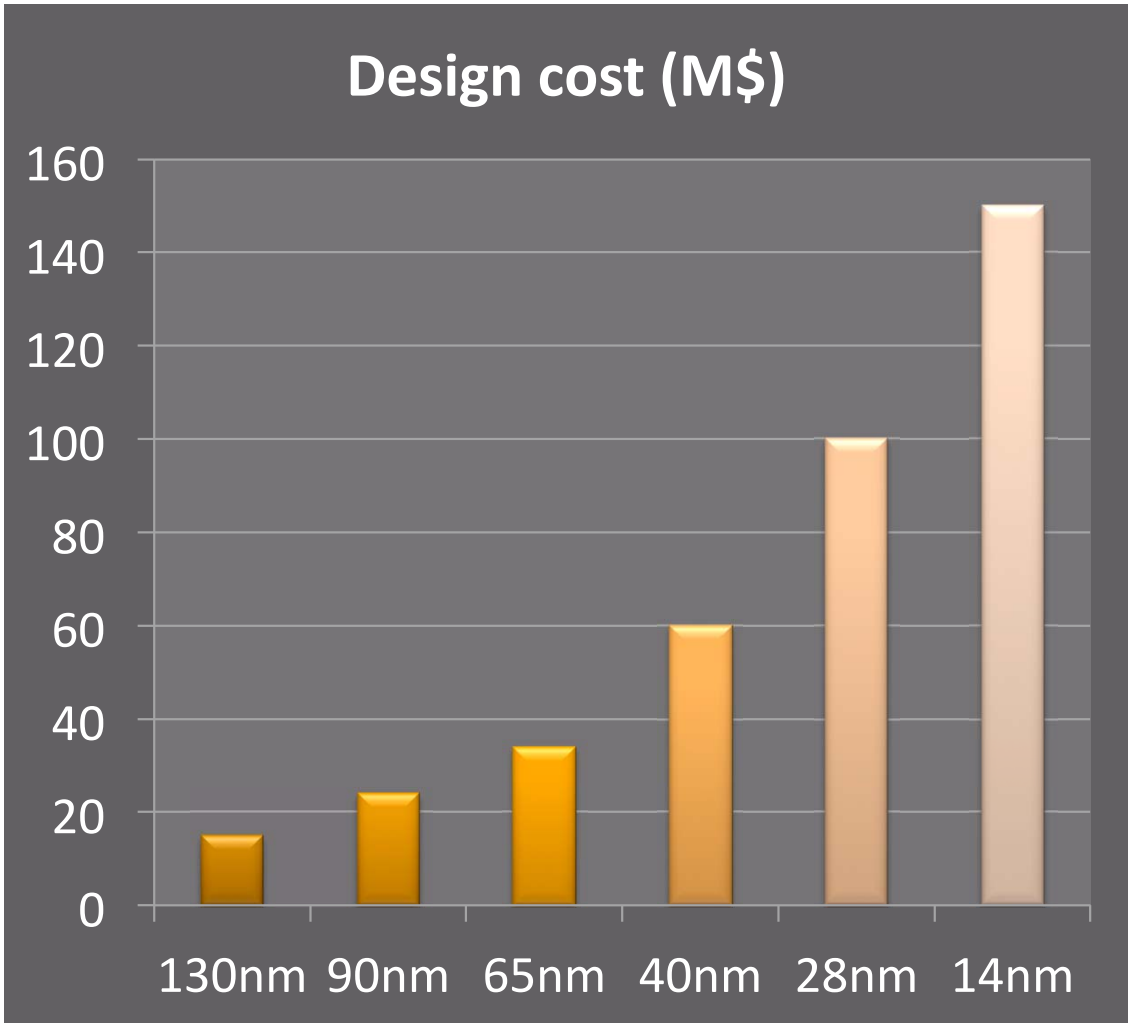


TECHNOLOGY TRENDS
INCREASED COST

- More complex process
- Challenges in nano-scale patterning
- 20 companies in 130nm
- 4 companies (alliances) in 14nm
- 7 Billion $ fab cost
- IC design cost explosion:

1 IC DESIGN
150 M$

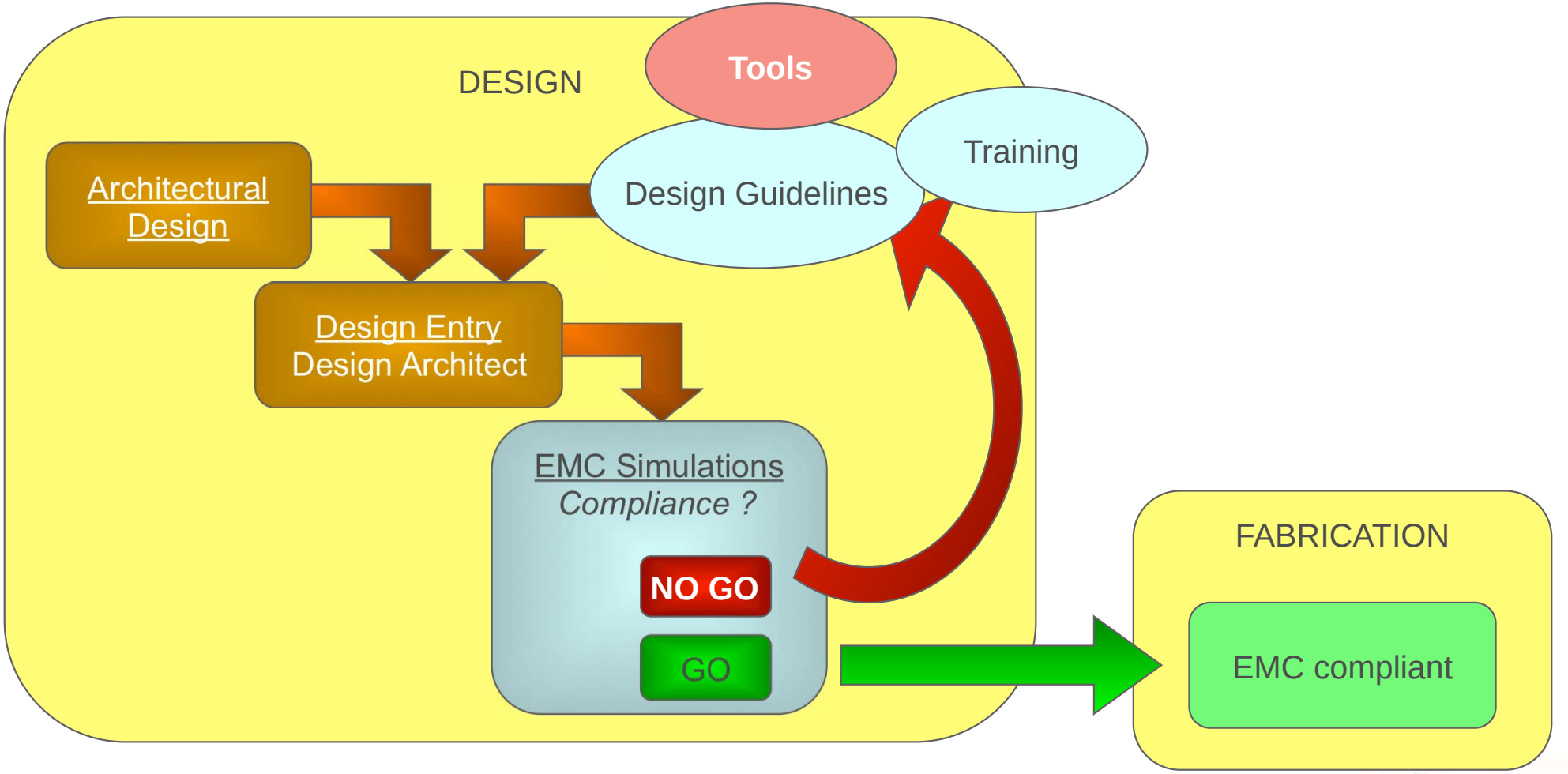
1 RUN ITERATION
10 M$



A. Manocha, Foundry driven innovation in the mobility era, Global Foundries, 2013

MOTIVATION

- **Lack of tools, guidelines and training in EMC of Integrated circuits, for improved EMC before fabrication**



WHAT IS IC-EMC

- A schematic editor
- An interface to Spice analog simulation
- A post-processor to compare simulated with measured spectrum
- An Electromagnetic solver for radiated field
- Freeware, online
- 250 pp documentation, 15 case studies
- 1-week trainings

Key tools

Spectrum analysis

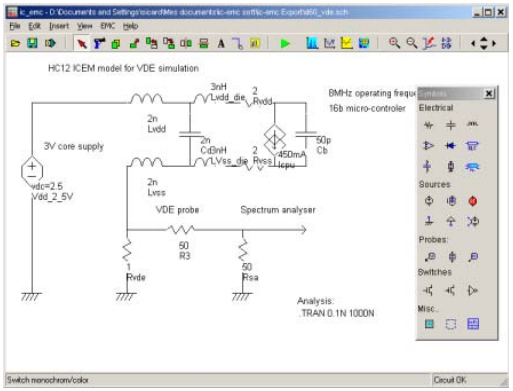
Near-field simulation

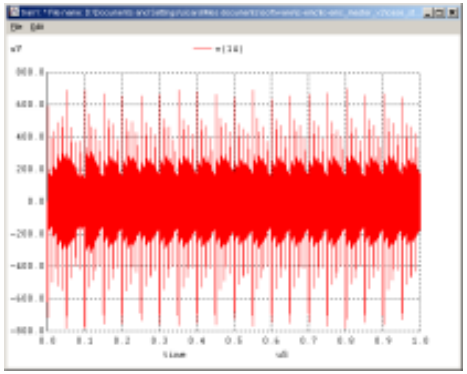
Immunity simulation

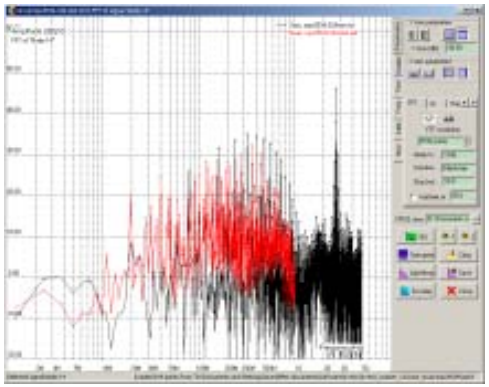
Impedance simulation

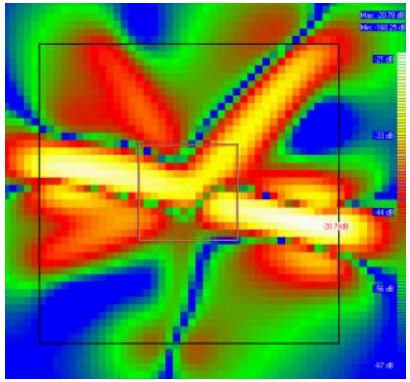
Smith Chart

IBIS interface









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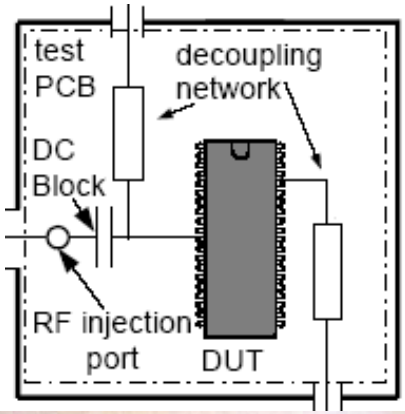
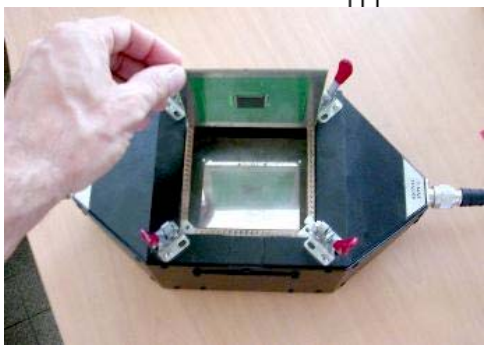
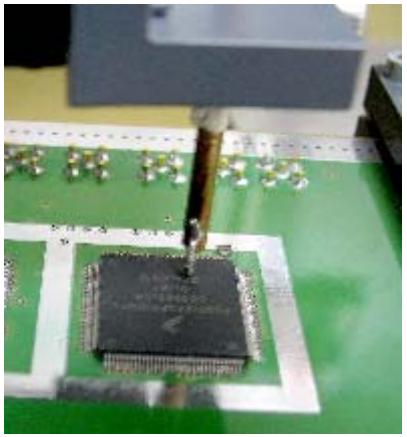
SUPPORTED STANDARD MEASUREMENT METHODS

- **IC-EMC is using simple models of standards EMC methods**
  - 1/150 Ω
  - TEM, GTEM
  - Near-field scan
  - Direct Power Injection
- **Maybe used for**
  - Emission
  - Immunity
- **These first-order models allow fast predictions upto 1GHz with reasonable accuracy**







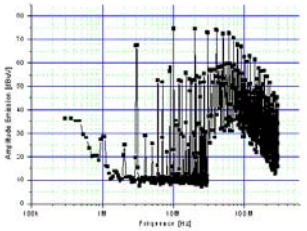
IEC

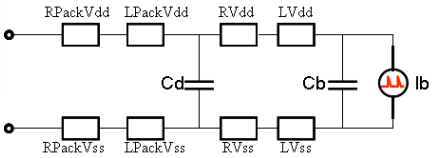
www.iec.ch

SUPPORTED STANDARD MODELLING METHODS

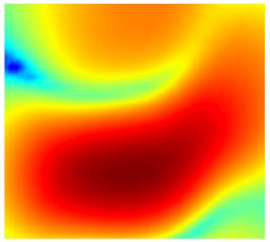
- **IC-EMC illustrates concrete application of IBIS, ICEM and ICIM models for EMC prediction**

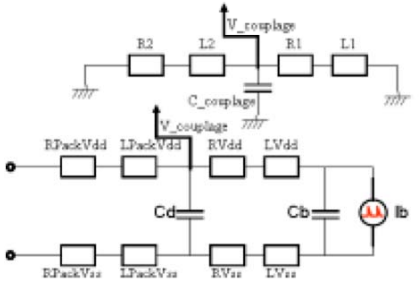
1. ICEM-CE - Conducted RF emission



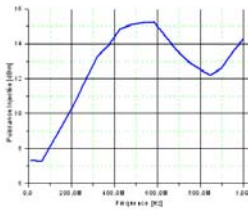


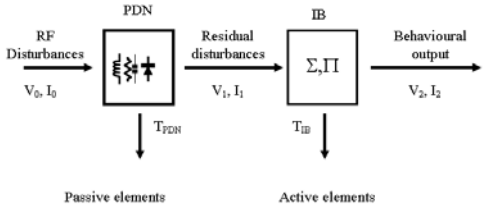
2. ICEM-RE - Radiated RF emission



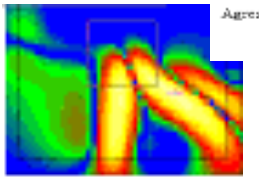


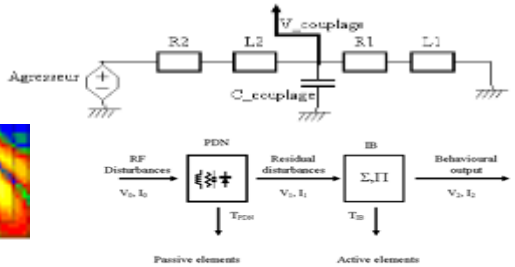
4. ICIM-CI - Conducted RF immunity





4. ICIM-RI - Radiated RF immunity





www.iec.ch

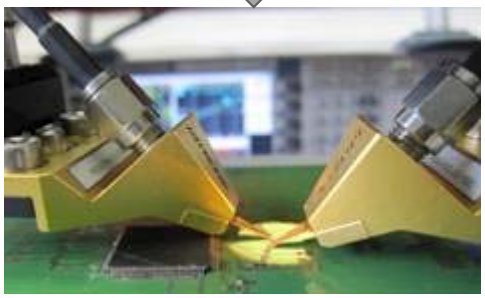
www.eda.org/ibis

EXAMPLE 1 – IMPEDANCE MODELLING

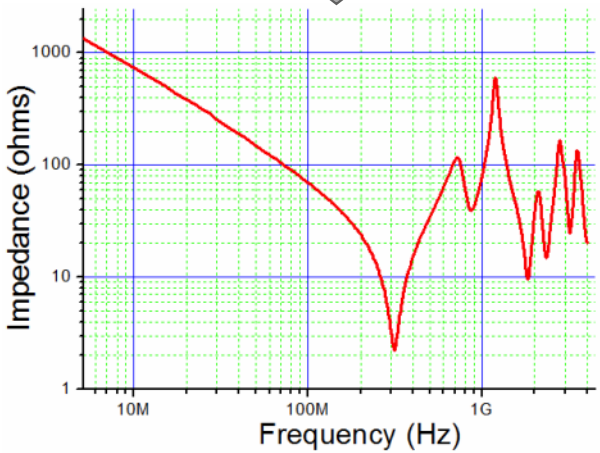
- **Z(f) measurements based on [s] using network analyzer and microwave probes**
- **Package pitch: 1mm down to 250µm**
- **Frequency of interest: 1 MHz – 10 GHz**

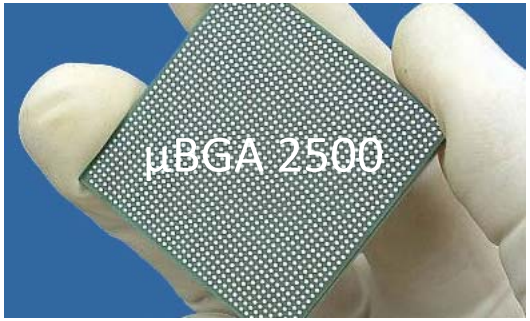
Vector Network Analyzer

GHz probes



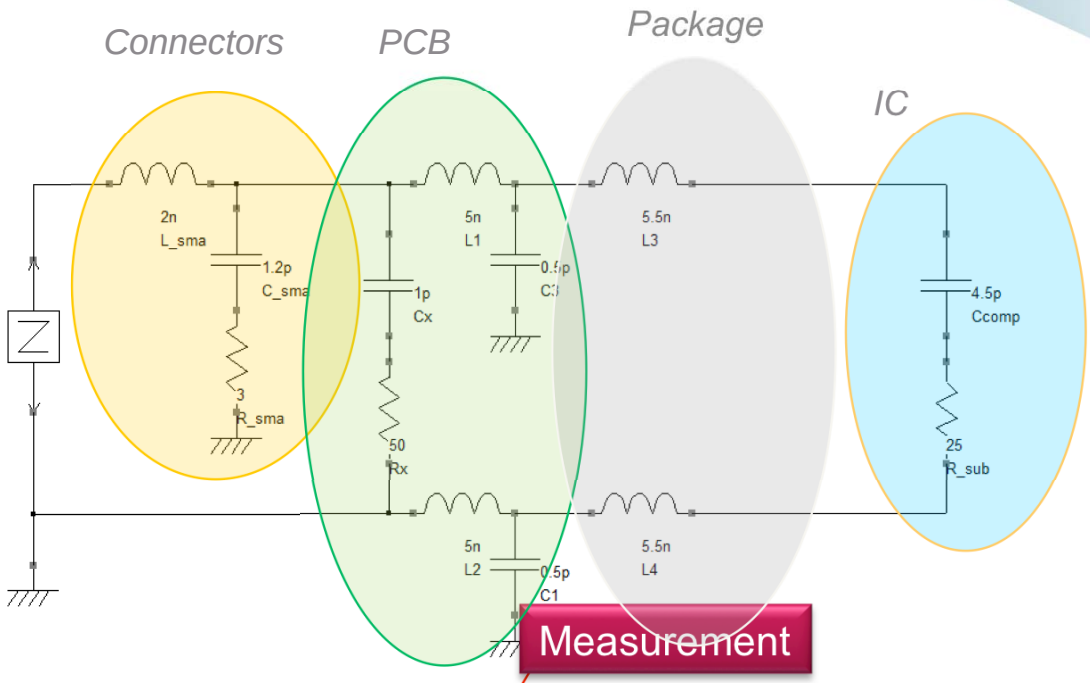
[s] Z(f)

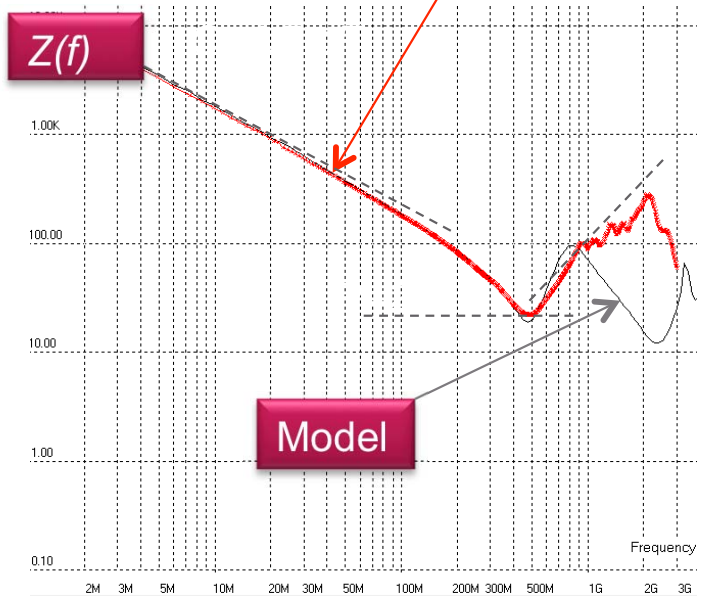




EXAMPLE 1 – IMPEDANCE MODELLING

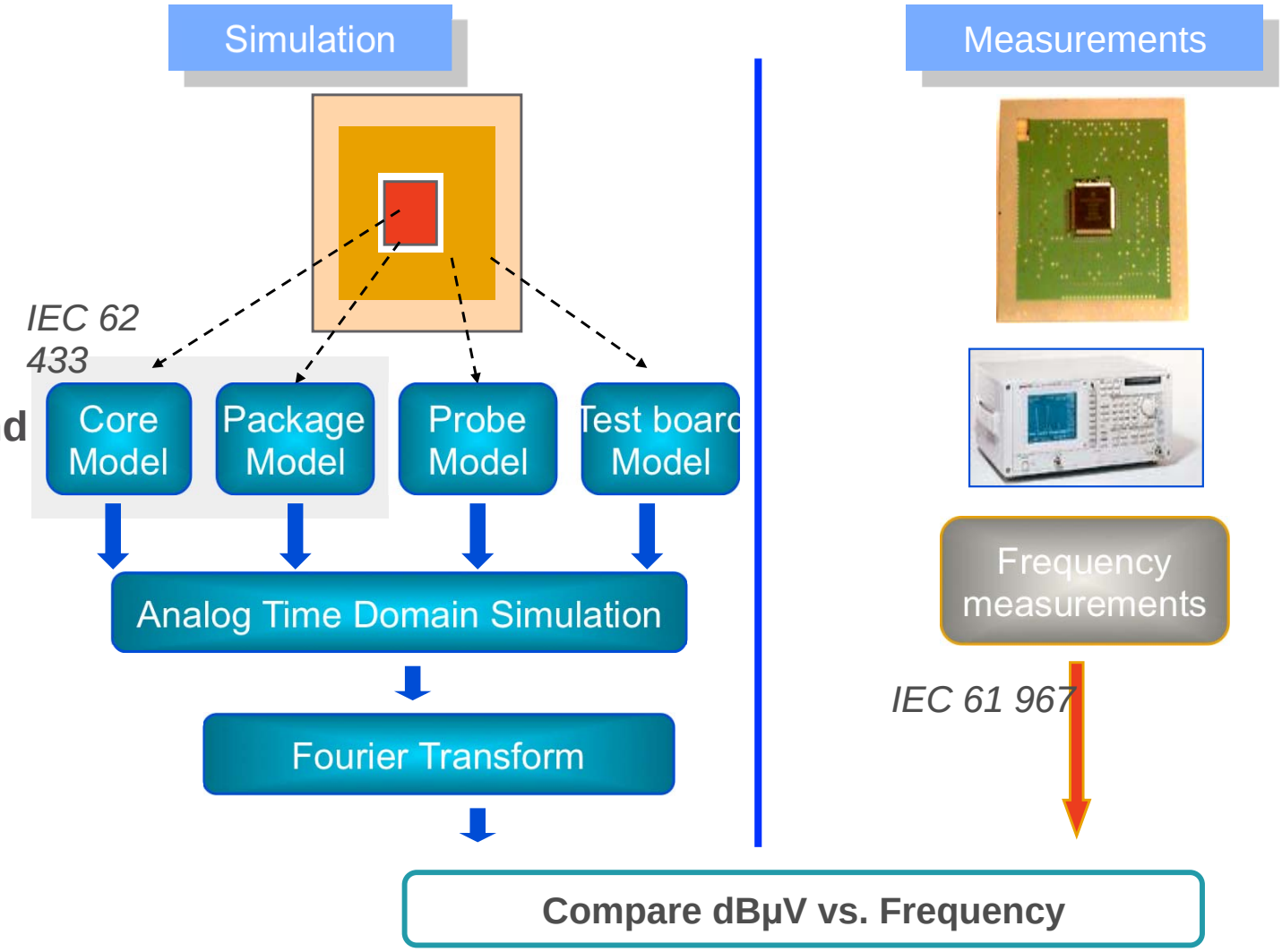
- Tune R,L,C based model from measured Z(f)
- Identify dominant parameters and to link the values to physical characteristics
- Package impedance
- On-chip impedance
- PCB tracks impedance
- Discrete R,L,C
- EMC probes





EXAMPLE 2 – PREDICT CONDUCTED EMISSION

- Build emission model
- Tune a model from measured spectrum (1/150 Ω method)
- Identify dominant parameters (I, L,C..) and to link the values to IC characteristics
- Number of gates
- On-chip decoupling
- Supply pairs



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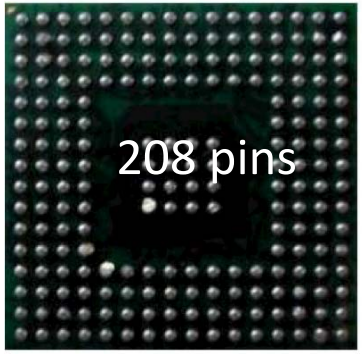
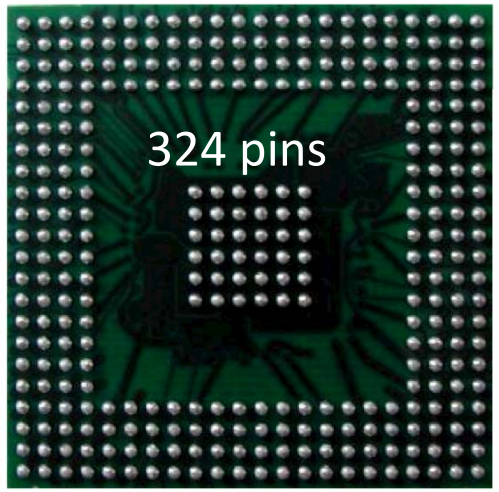
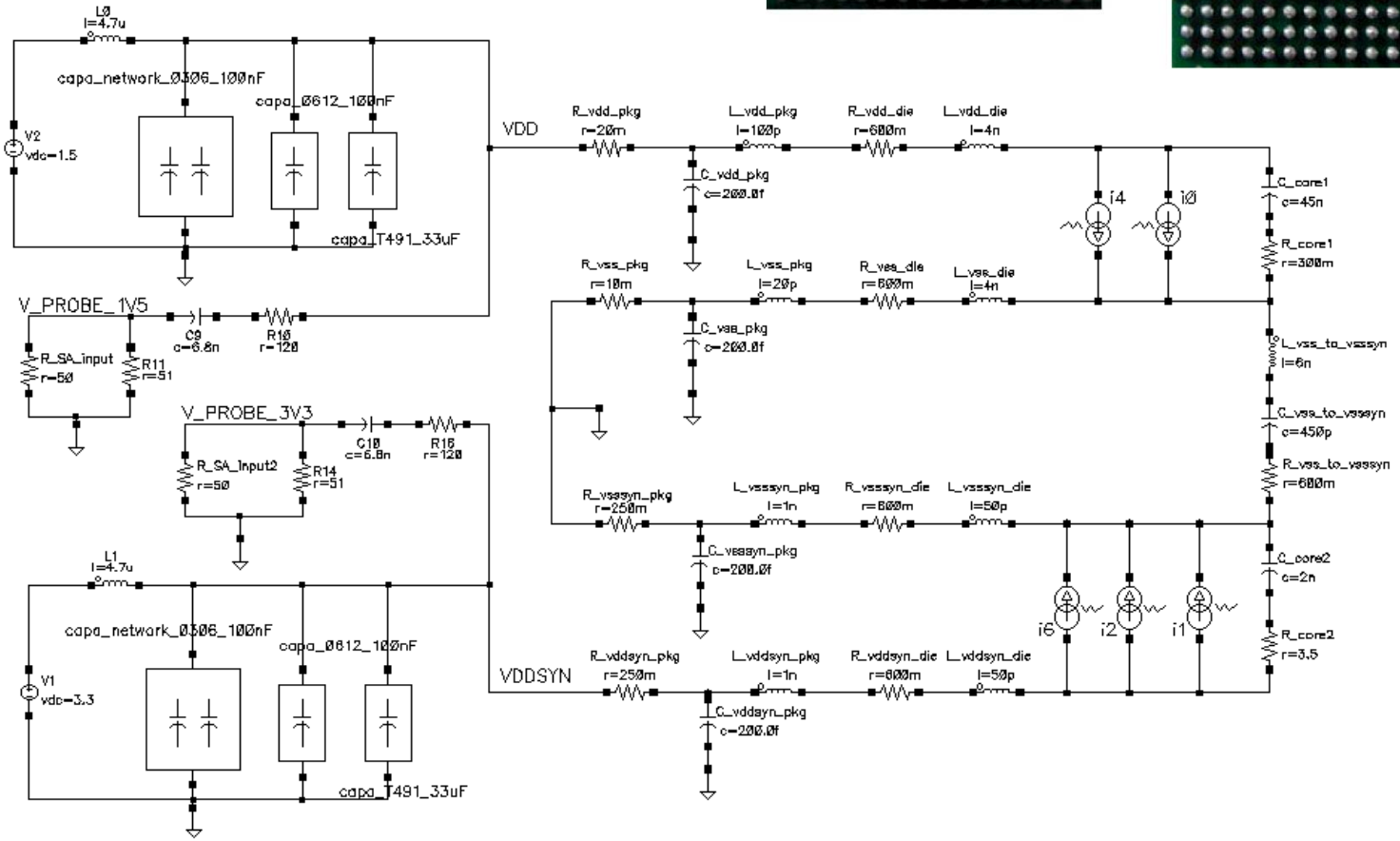
EXAMPLE 2 – PREDICT CONDUCTED EMISSION

- Freescale MPC 5534 case study
- One core, two BGA package versions (208, 324 pins)

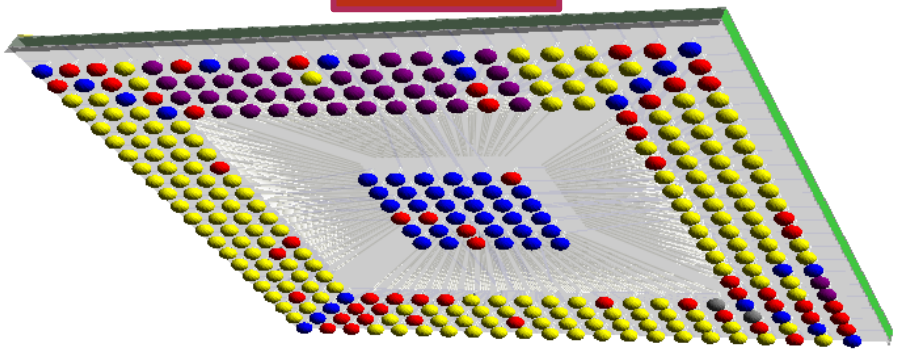




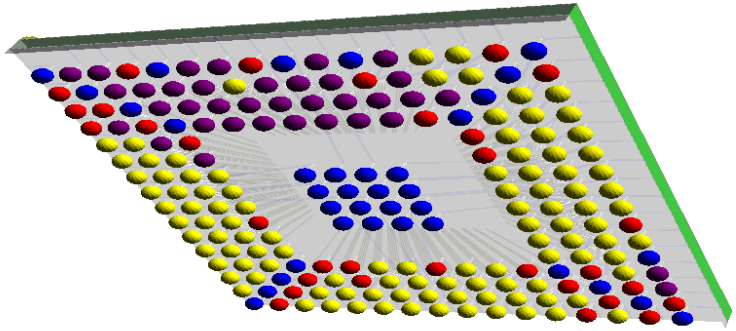


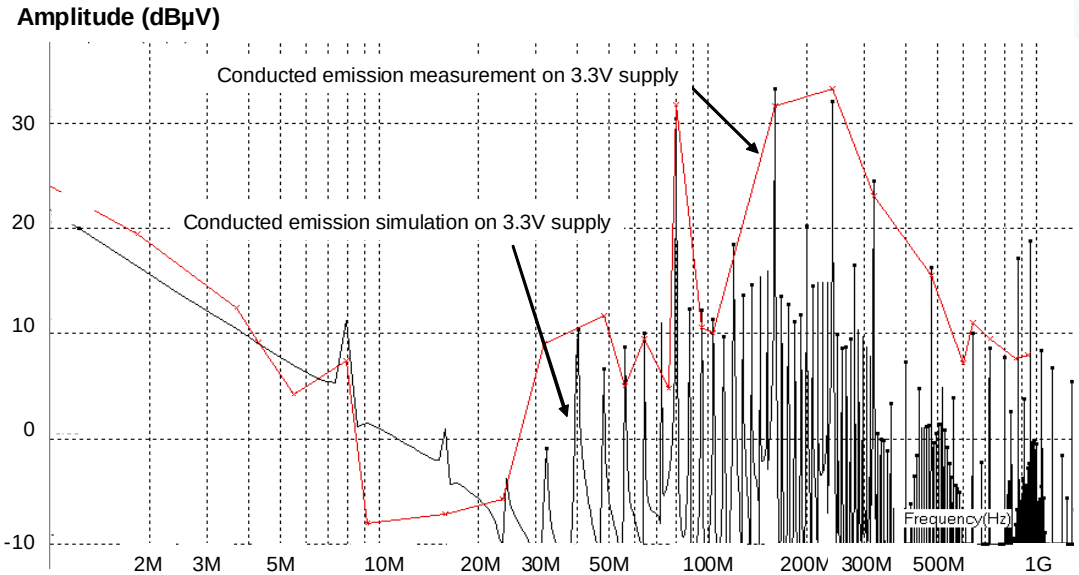
EXAMPLE 2 – PREDICT CONDUCTED EMISSION

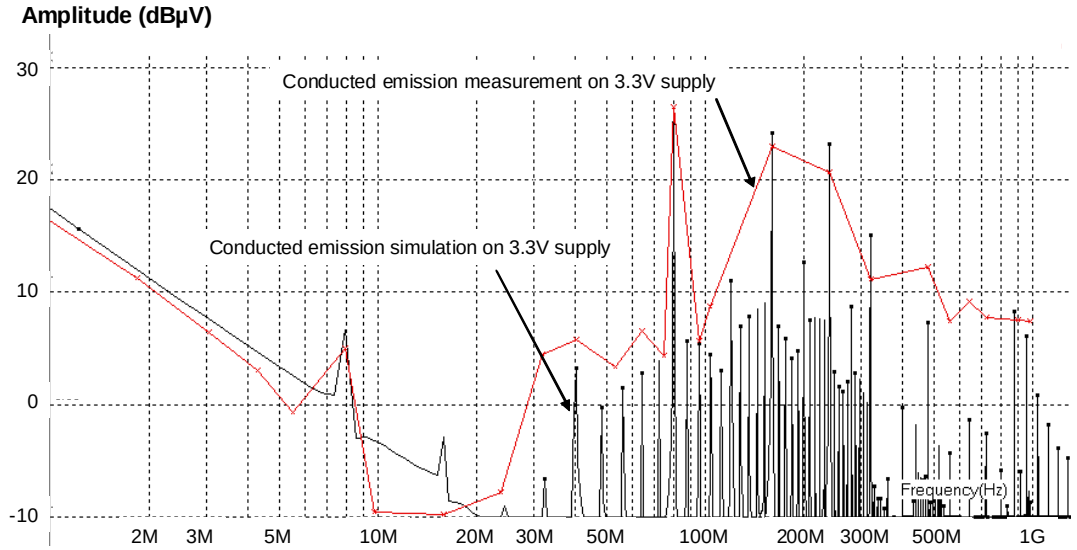
324 pins



208 pins



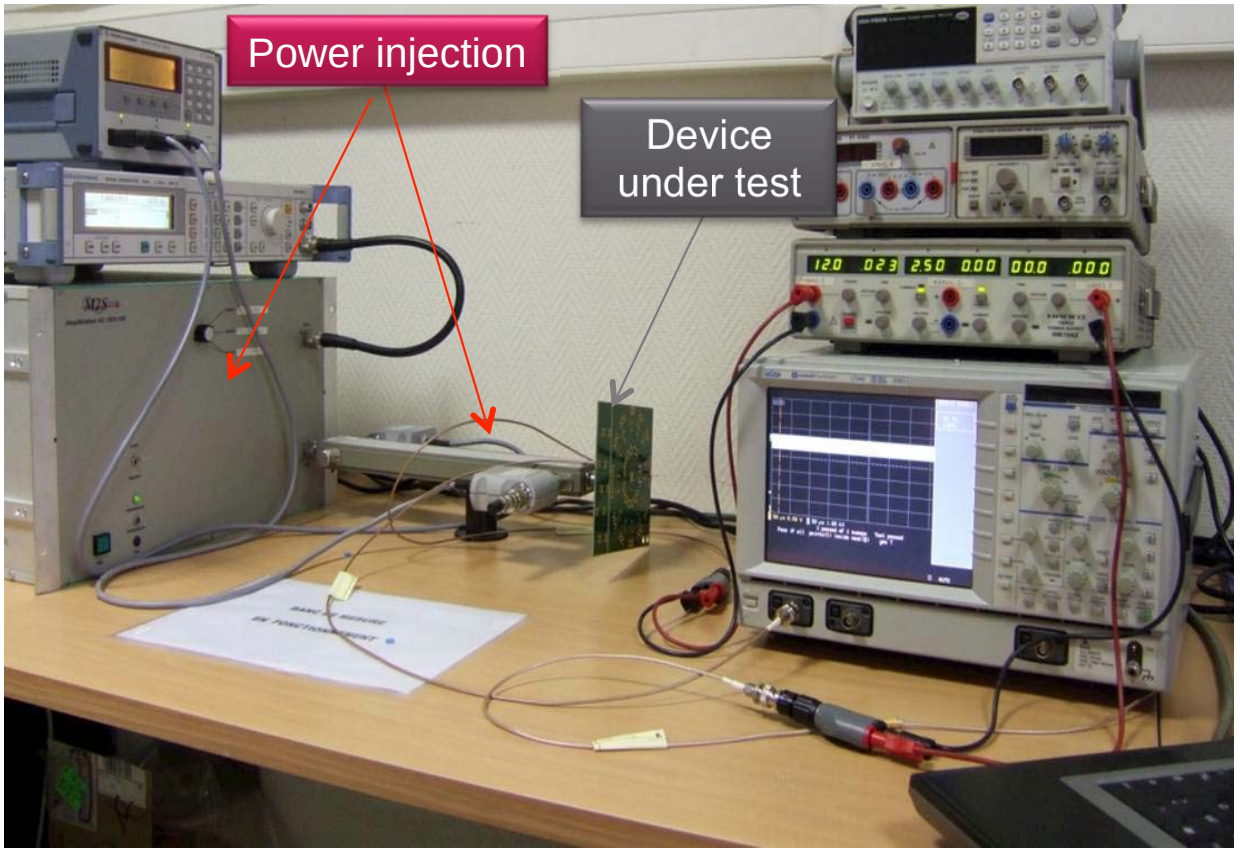




E. Rogard, Characterization and Modelling of Parasitic Emission of a 32-bit Automotive Microcontroller Mounted on 2 Types of BGA, EMC Austin 2009

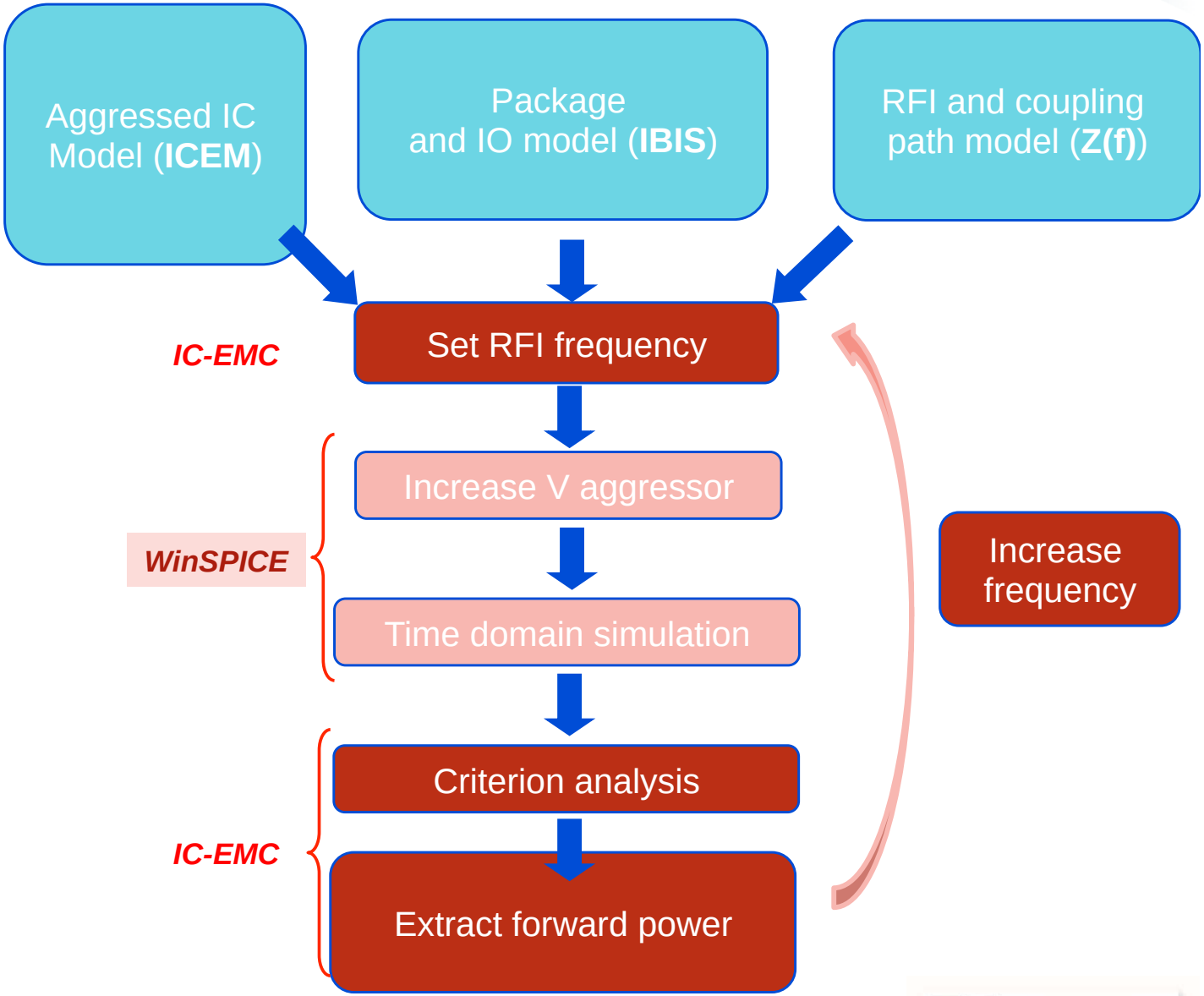
EXAMPLE 3 – PREDICT IMMUNITY

- **Immunity modelling does not concern only the IC**
- **The power injection setup must be modeled with care**
  - Power amplifier
  - Coupler
  - Forward, reflected Power
  - PCB Injection path
  - Coupling to IC
- **The Input/output structures of the IC are critical**
- **The IC failure criteria is an opened issue**

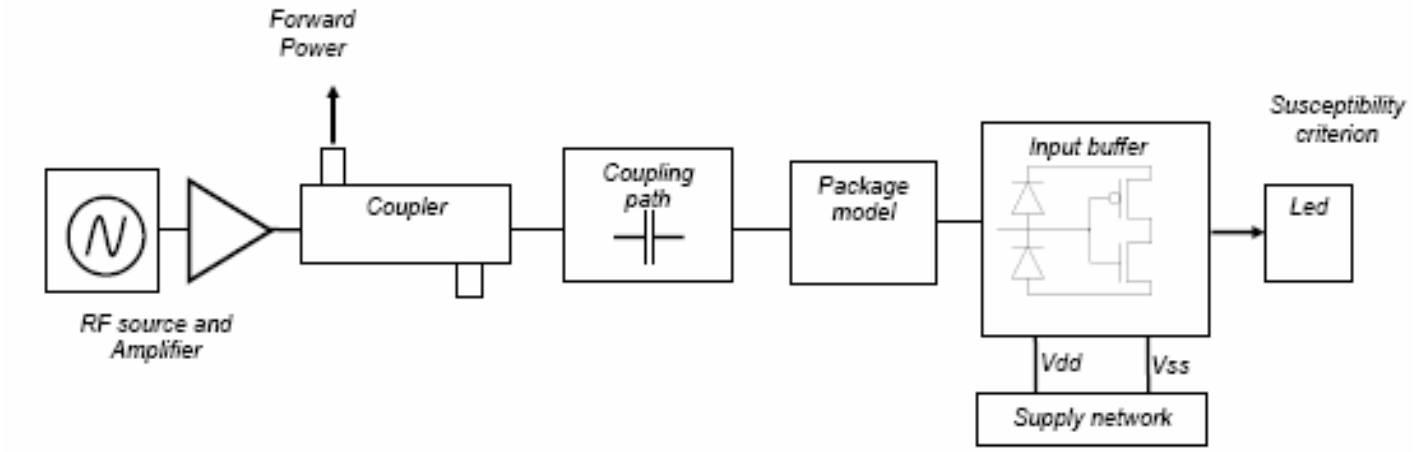


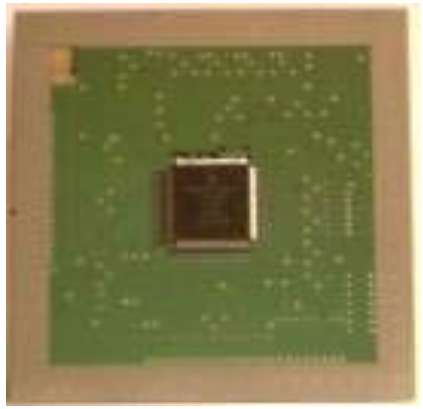
EXAMPLE 3 – PREDICT CONDUCTED IMMUNITY

- **A model can be tuned from measured immunity measurement (DPI method)**
- **Exploit coupler, power extraction, susceptibility criteria.**
- **IC-EMC eases the iterative simulation**

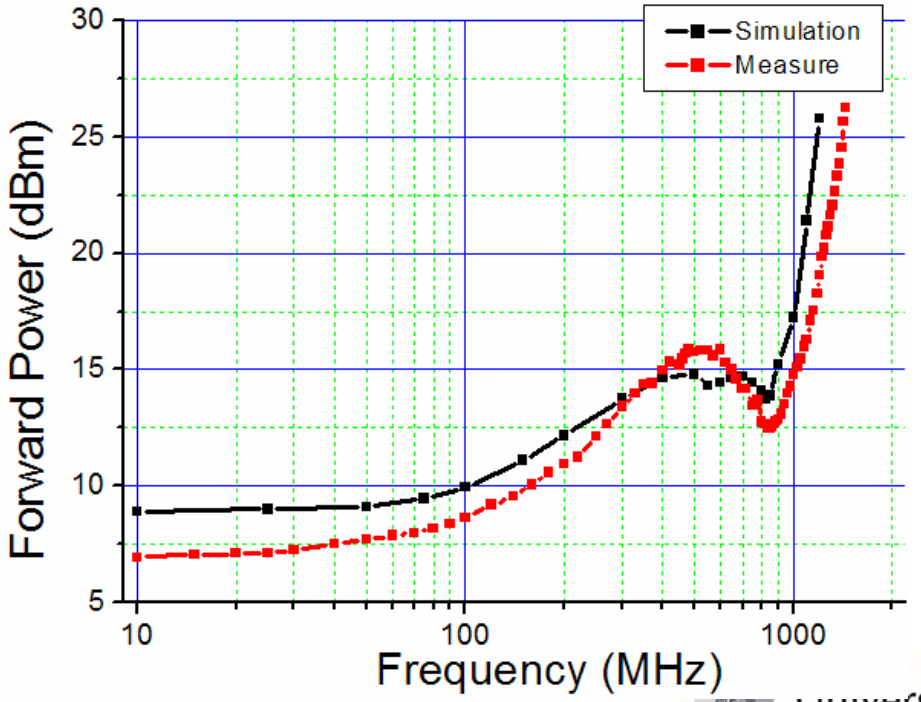


EXAMPLE 3 – PREDICT CONDUCTED IMMUNITY

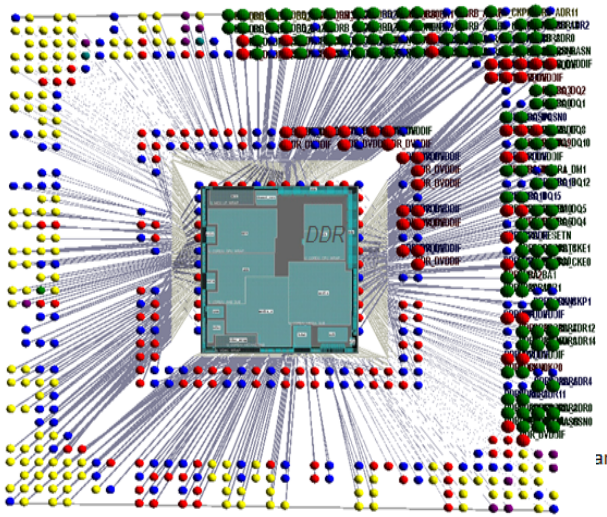


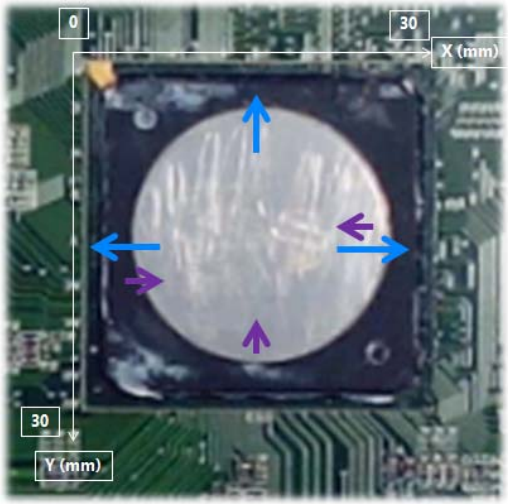


- 16 bit micro-controller
- Direct power injection
- Input buffer aggression
- Sinusoidal mode
- Simulation criterion: Logical change of input buffer

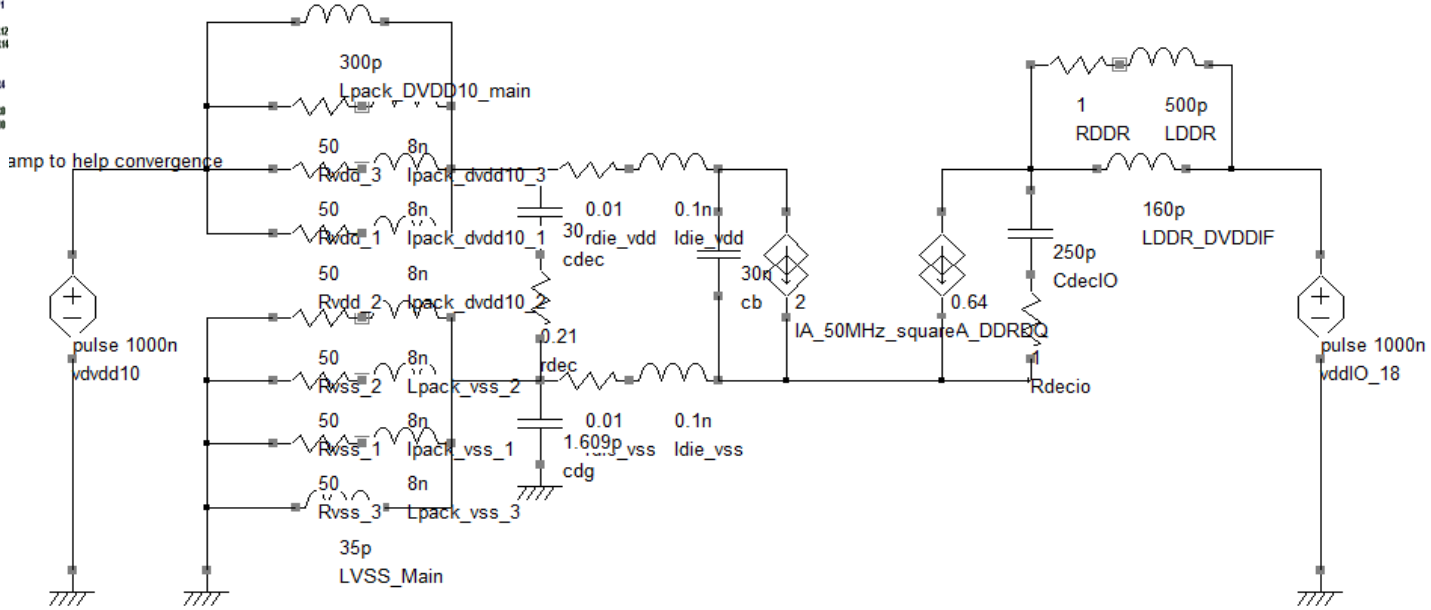


EXAMPLE 4
RADIATED EMISSION





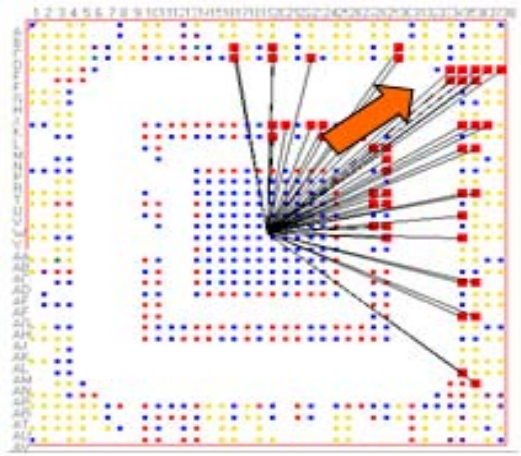
- Radiating elements representing local magnetic field sources, associated to inductances
- Extreme simplification of thousands of elementary sources



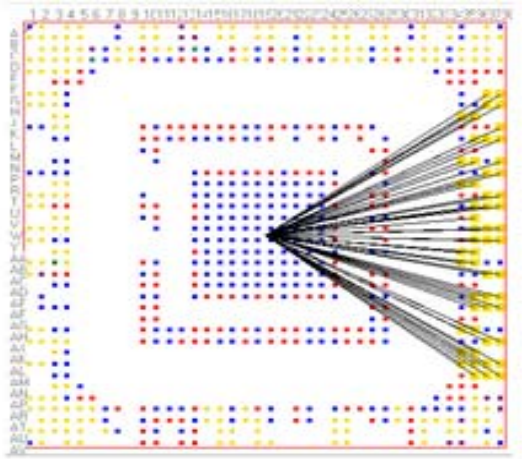
EXAMPLE 4
RADIATED EMISSION

- Power domain floorplan analysis enables to visalize unbalanced networks
- Risk of loops and radiation

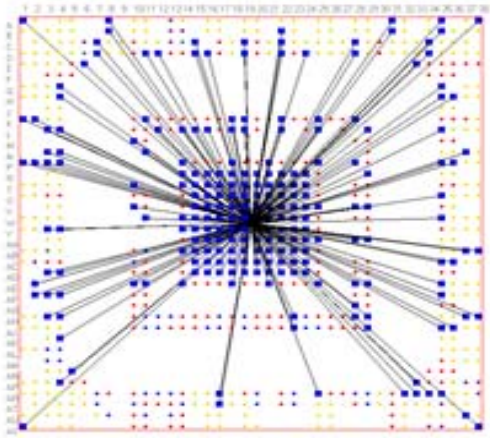
Supply: DDR_DVD DDIF



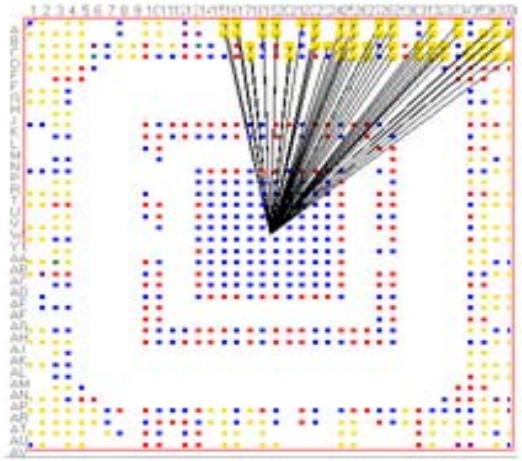
DDRA I/Os



Ground of DDR

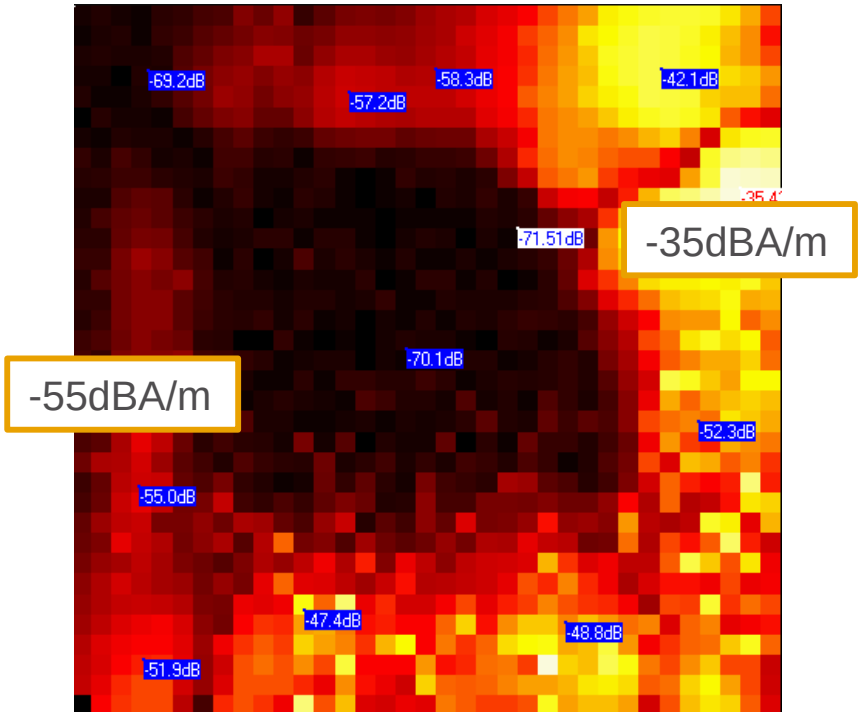


DDRB I/Os

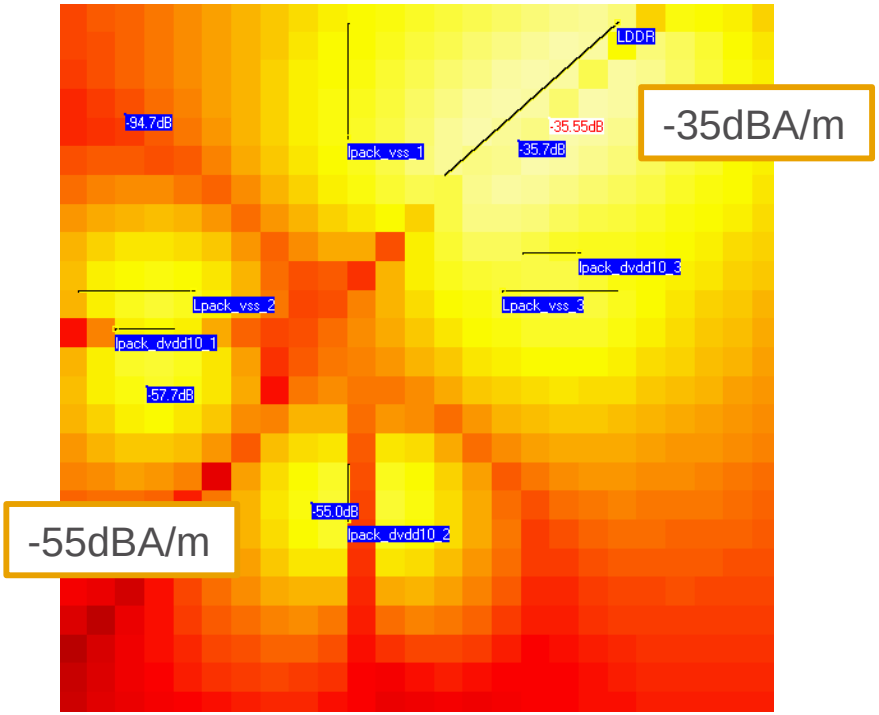


EXAMPLE 4
RADIATED EMISSION

- **NFS measurement vs simulation of Hz of a System-on-chip with DDR supply network**



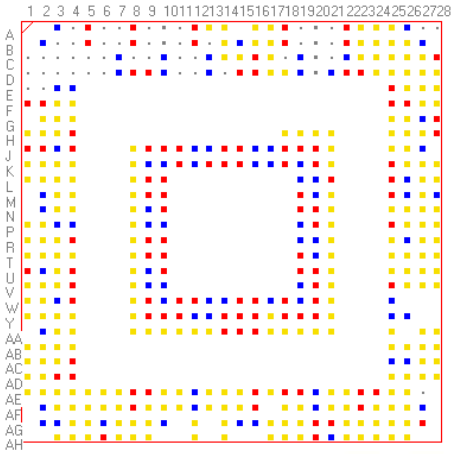
(a) measurement



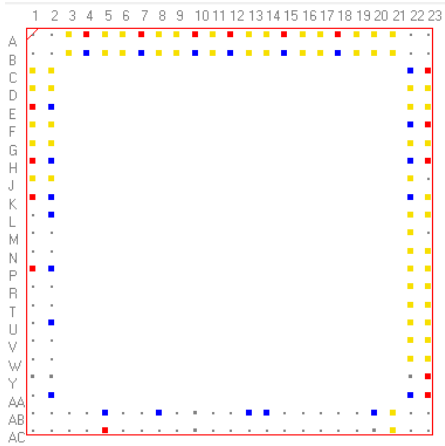
(b) simulation

EXAMPLE 5
3D PACKAGE ON PACKAGE

- **Merge of two IBIS of different ICs. SI/PI prospective analysis**

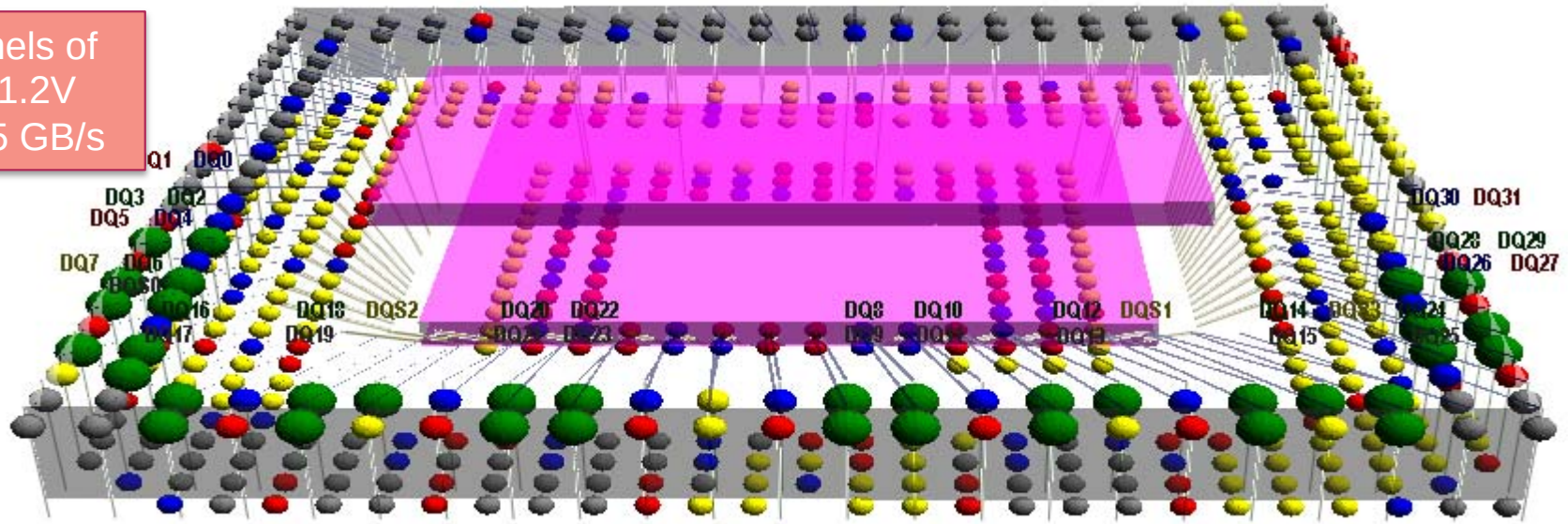


Lower BGA to board (0.4mm pitch)



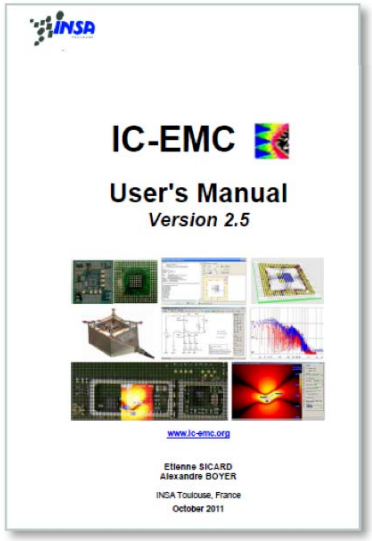
Upper BGA to memories (0.5mm pitch)

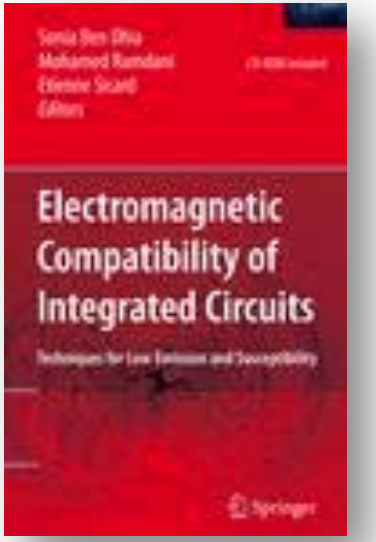
2 channels of 32-bit 1.2V DDR3, 5 GB/s

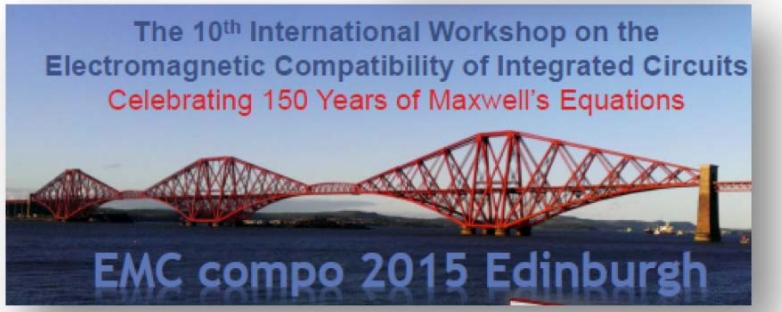


CONCLUSION

- An environment for EMC prediction at IC level and trainings has been developed
- The IC-EMC tool is a freeware
- Several IC case study available (measurements, models)
- Continuing education in EMC of ICs based on measurements & simulations
- Close contact with industry for case-study analysis







www.emccompo.org, Nov. 2015

Tool, manual, slides online at www.ic-emc.org

INSA INSTITUT NATIONAL DES SCIENCES APPLIQUÉES TOULOUSE

DEPARTEMENT DE GENIE ELECTRIQUE ET INFORMATIQUE

Merci pour votre attention

Université de Toulouse